

Compal confidential

PCA31 Schematics Document

Intel Pentium Dual Core Processor + GMCH G41+ ICH7

2010-07-14

REV: 0.3

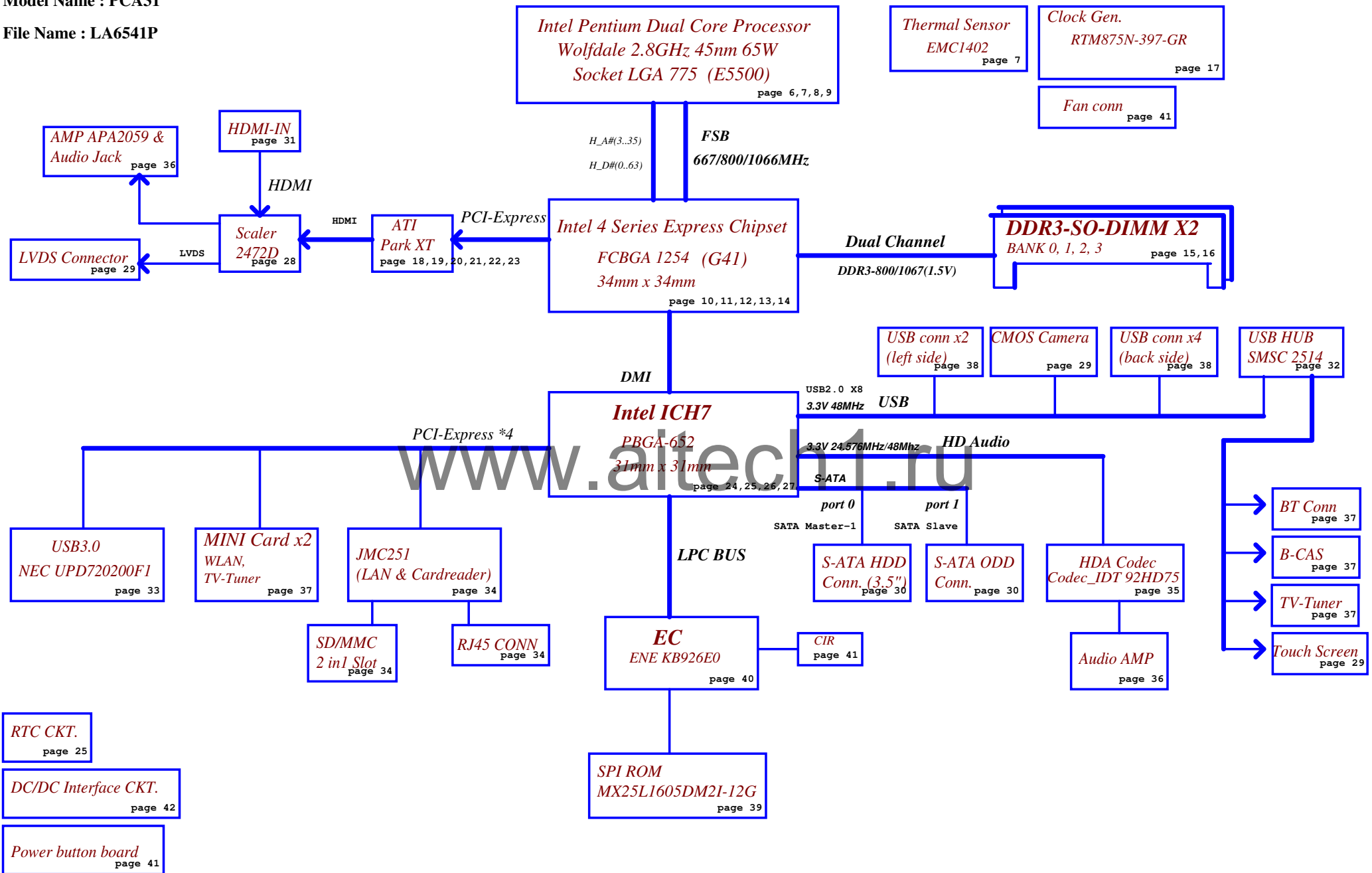
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				Cover Sheet	

Compal Confidential

Model Name : PCA31

File Name : LA6541P

INTEL 4 series



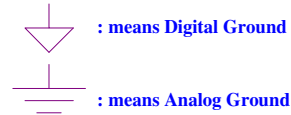
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Voltage Rails

○ MEANS ON X MEANS OFF

power plane State	B+	+5VALW +3VALW +1.2VALW	+1.5V	+5VS +3VS +1.5VS +VCCP +CPU_CORE +12VS +1.2V_VTT +0.75VS +3VS_DELAY +GPU_CORE +1.8VS_DELAY +1.0VS
S0	○	○	○	○
S1	○	○	○	○
S3	○	○	○	X
S5 S4	○	○	X	X

Symbol Note :



Layout Notes

CONN@ : means connector
 NS@ : means NS vendor
 SMSC@ : means SMSC vendor
 @ : means just reserve , no build
 45@ : Install when 45 level Assy
 X76@: VRAM vendor
 USB30@: means USB3.0

I2C / SMBUS ADDRESSING

DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	10100000
DDR SO-DIMM 1	A4	10100100
CLOCK GENERATOR (EXT.)	D2	11010010

EC SM Bus1 address

Device	HEX	Address
Scaler	TBD	TBD

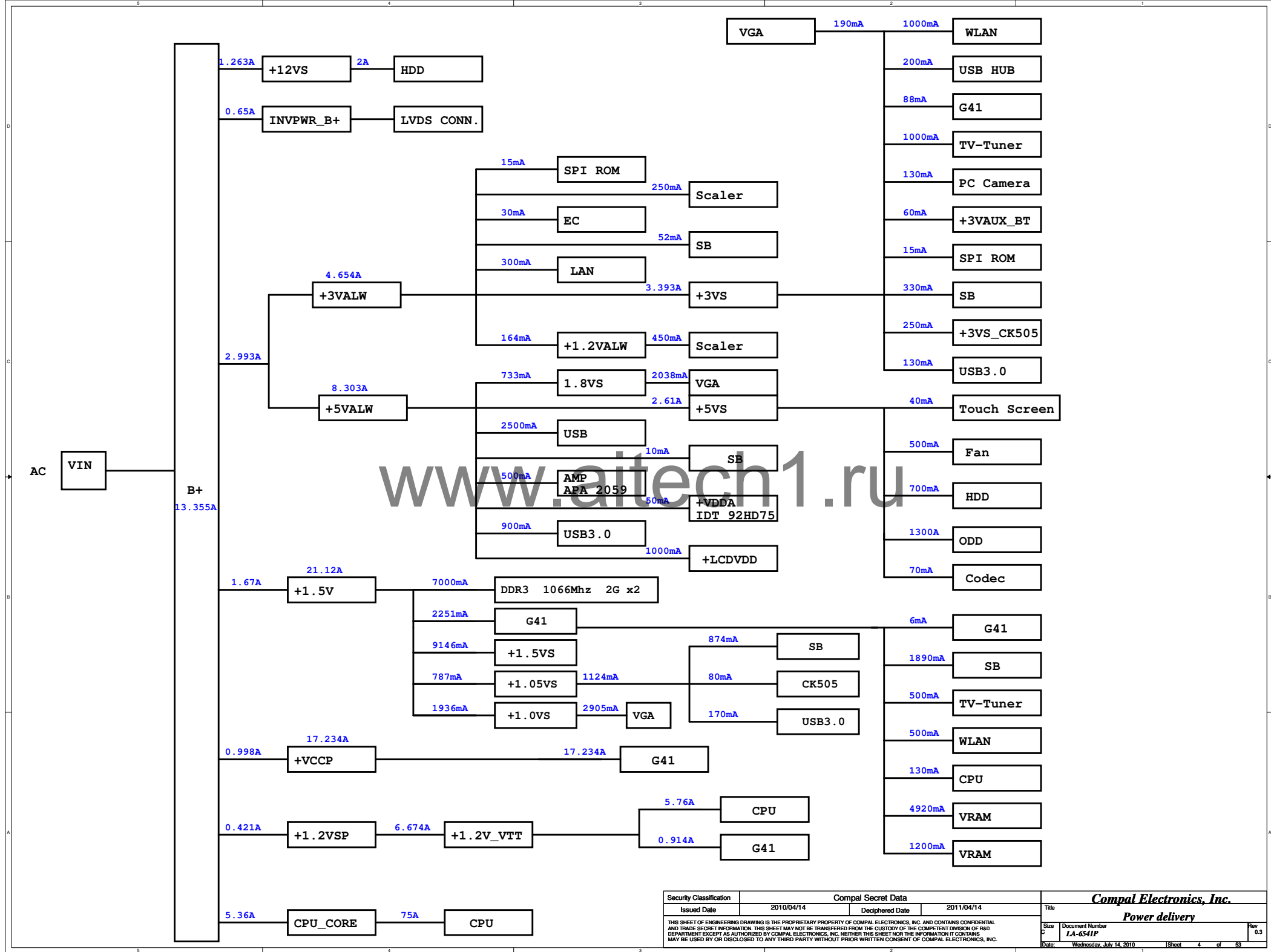
EC SM Bus2 address

Device	HEX	Address
CPU	98H	1001 100X b
GPU-SMB	41H	0100 0001 b

SMBUS Control Table

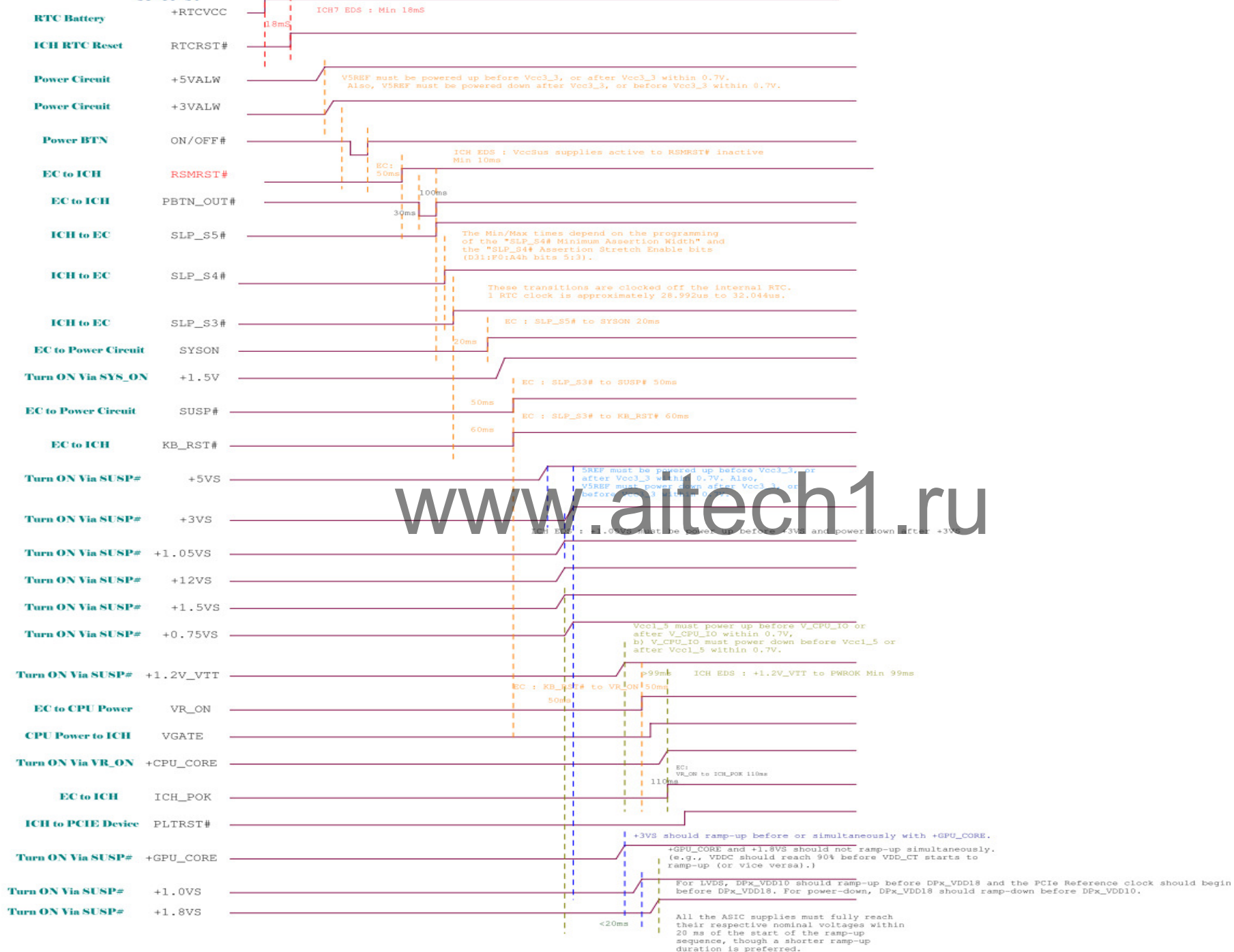
	SOURCE	Scaler	THERMAL SENSOR CPU	SODIMM I / II	VGA	LCD	HDMI IN	CLK CHIP	MINI CARD Slot 1
EC_SMB_CK1	KB926	V	X	X	X	X	X	X	X
EC_SMB_DA1	KB926	X	V	X	X	X	X	X	X
EC_SMB_CK2	KB926	X	V	X	X	X	X	X	X
EC_SMB_DA2	KB926	X	V	X	X	X	X	X	X
HDMI_TV_SCLK	Scaler	X	X	X	X	X	V	X	X
HDMI_TV_SDATA	Scaler	X	X	X	V	X	X	X	X
HDMICLK_S	Scaler	X	X	X	V	X	X	X	X
HDMIDAT_S	Scaler	X	X	X	V	X	X	X	X
ICH_SMBCLK	ICH7	X	X	V	X	X	X	V	X
ICK_SMBDATA	ICH7	X	X	V	X	X	X	V	X
EC_RX_P80_CLK	KB926	X	X	X	X	X	X	X	V
EC_TX_P80_DATA	KB926	X	X	X	X	X	X	X	V

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PCA31 Power Sequence

S5 to S0



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<17> CLK_CPU_BCLK_R
<17> CLK_CPU_BCLK#_R

Add R425/C100 for ESD request
Place close to JCPU1

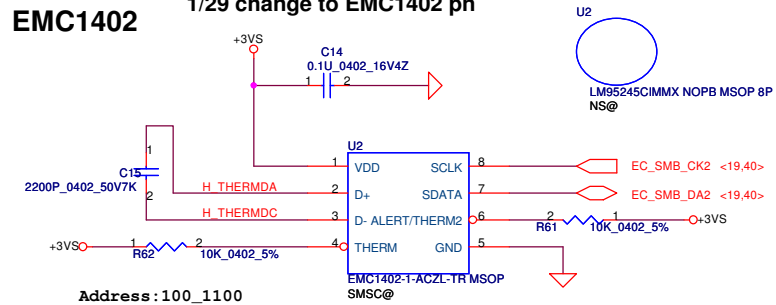
<26> XDP_DBRESET#
0528 Change C100 from
100p to 0.1u for noise

Change R40 from mount to @ 0416

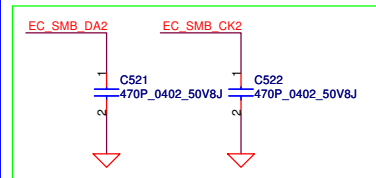
H THERMDA R43 1 2 0 0402 5% AL1
H THERMDC R44 1 2 0 0402 5% AL1
VCCSENSE R47 1 2 0 0402 5% AN3
VSSSENSE R48 1 2 0 0402 5% AN4
VCCSENSE R49 1 2 0 0402 5% AN5
VSSSENSE R50 1 2 0 0402 5% AN6
95W Yorkfield : Stuff R47,R48
65W Wolfdale : Stuff R49,R50

Following KHLB2

EMC1402 1/29 change to EMC1402 pn

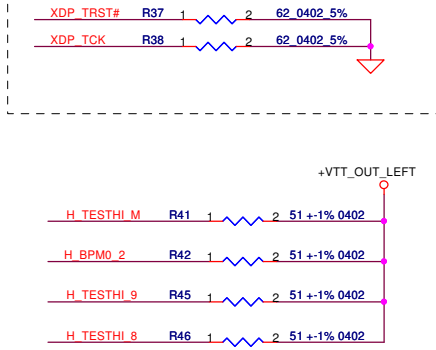
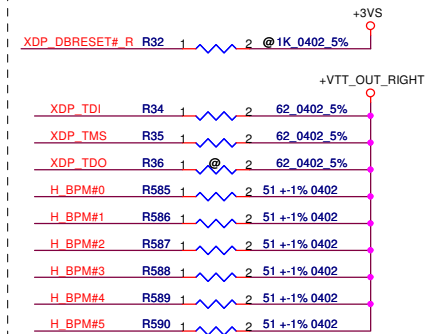


0713 Add C521/C522 for switching noise

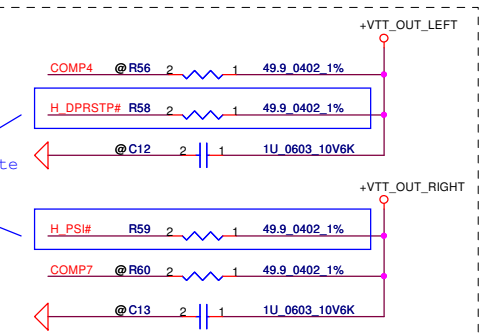


G41 PDG recommend to route
49.9 ohm to V_FSB_VIT

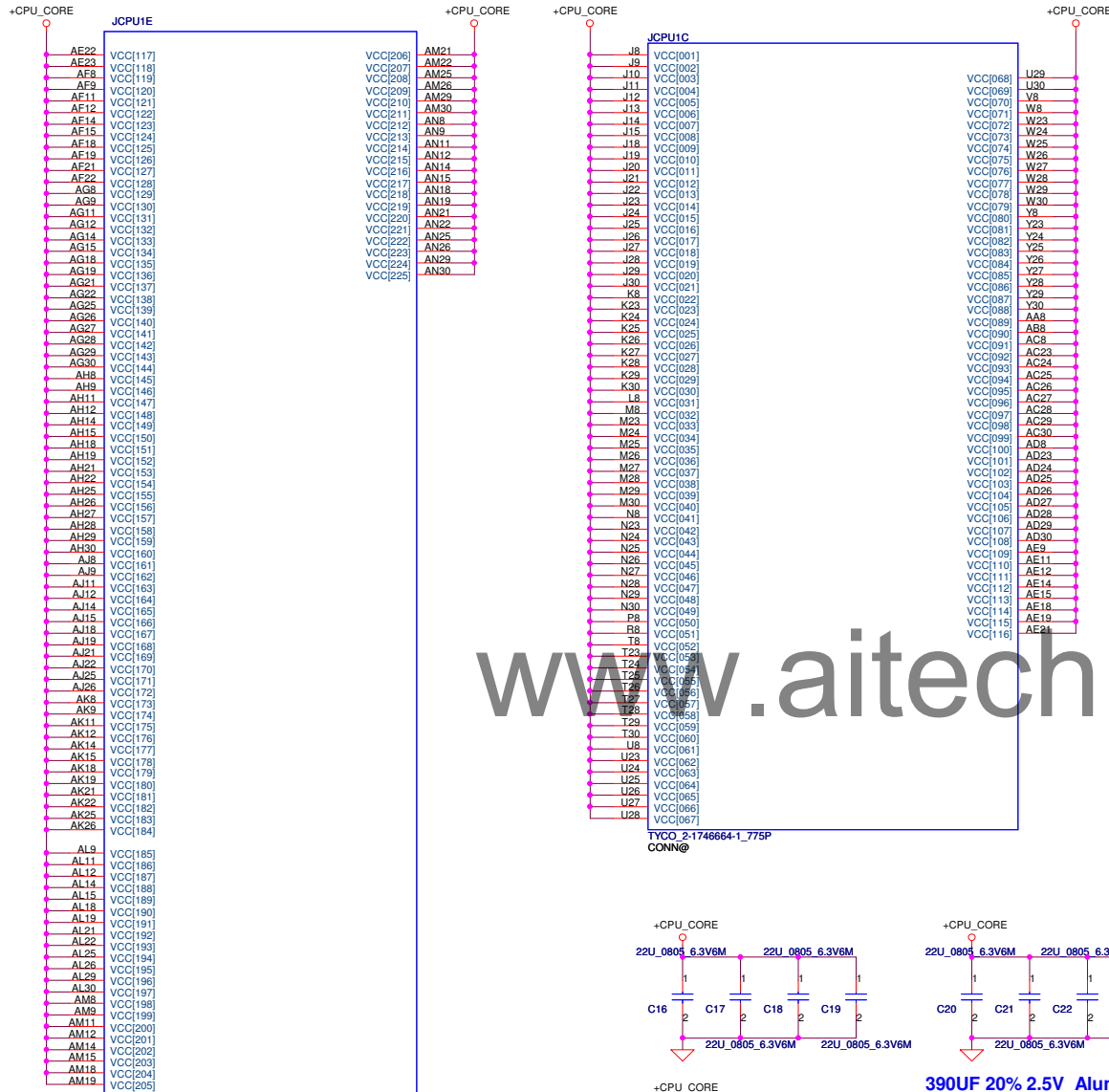
XDP Reserve



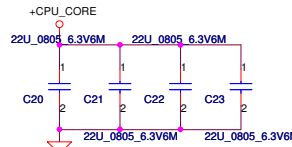
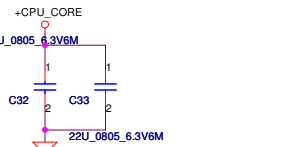
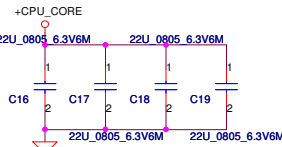
Layout Note:
COMP8 trace length < 1.2"
Trace width / space is 15/14



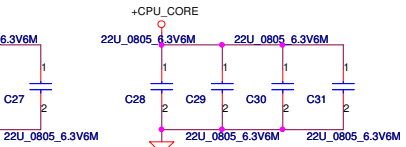
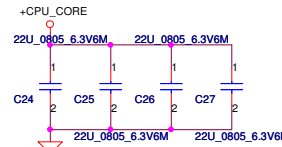
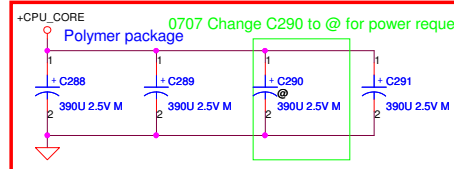
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				Dual Core (2/4)			
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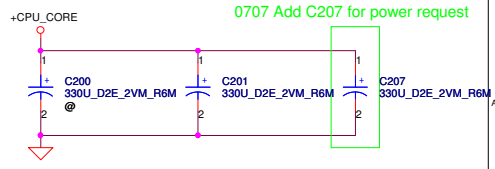
TYCO 2-1746664-1_775P
CONN@



390UF 20% 2.5V Alum x4 for +CPU_CORE
Change C288-C291 Value from 330U 6.3V_M to 390U 2.5V_M
6.3"H5.7 10mQ max.

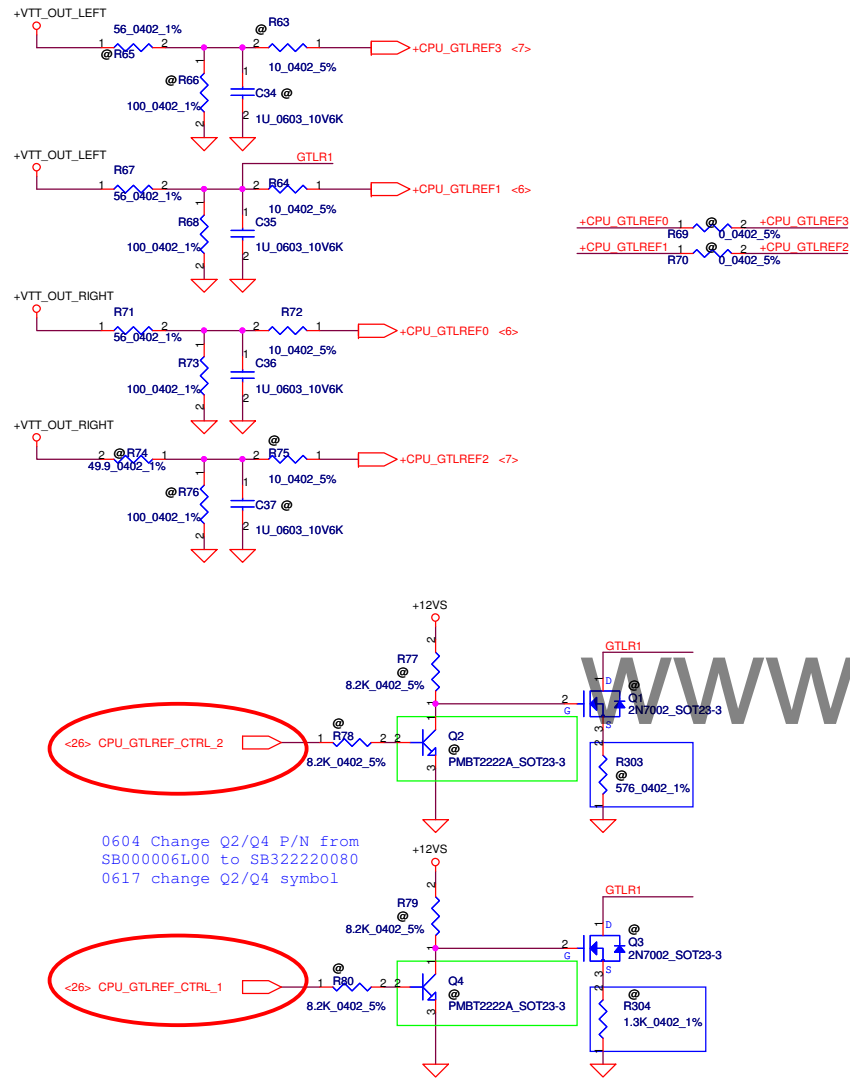


0510 Change C200/C201 from 470u to 330u.
P/N change to SGA00002U00 6mQ
0601 change P/N to SGA00001Q80



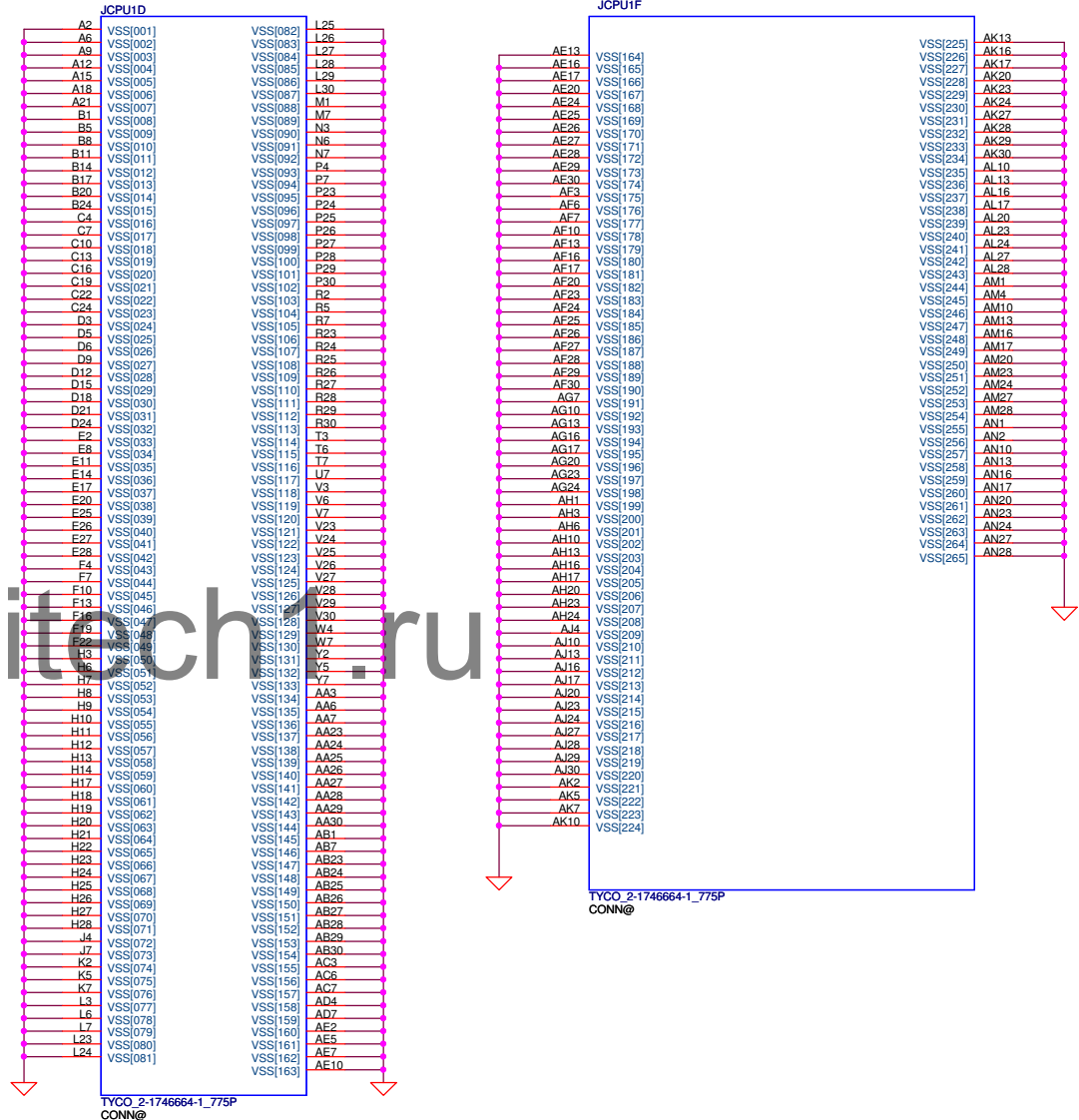
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CPU GTLREF



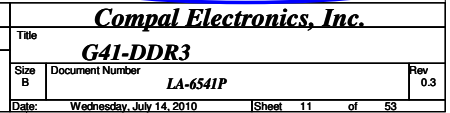
Recommended GPIO values for variable GTLREF voltage divider

CPU_GTLREF_CTRL_2	CPU_GTLREF_CTRL_1	Ratio Set
1	1	0.67
1	0	0.65
0	1	0.63
0	0	0.615

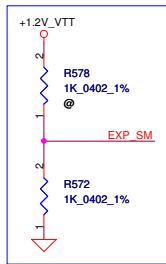


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								Dual Core [4/4]			
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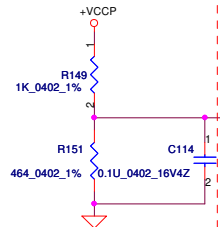
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Reserve R572 for EXP_SM use SDVO or PCIE card 0502
Reserve R578 for EXP_SM use SDVO or PCIE card 0504

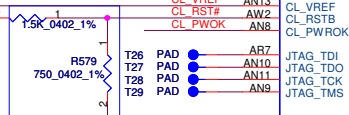
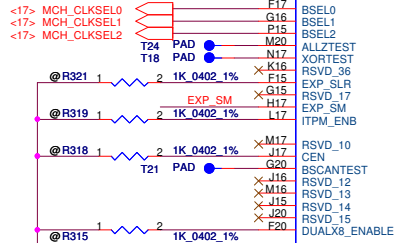


Checking ICH7 without ME



Change R151 P/N from SD034499080 to SD000000JH80
Value from 499_0402_1% to 464_0402_1%

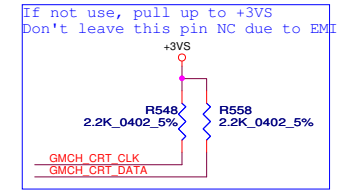
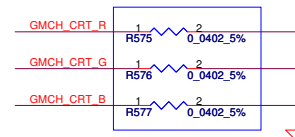
0517 Delete R316, R317, R320, T19, T20, T22, T23, T25



Add divider network for CL_RST# 0503

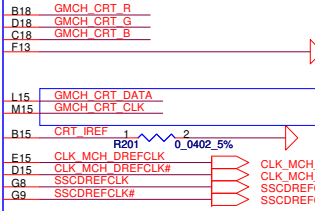
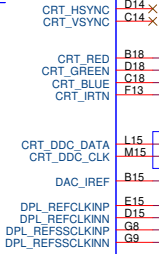
0517 Delete T30-T38

Change GMCH P/N to SA000042U10 for T88



For P-series MCH

Stuff R225/R266 for non-graphics skus
Stuff R226/R235 if not support display port 0416

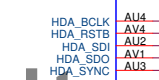


0518 change from 100ohm to 0ohm

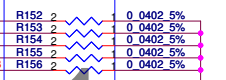


0527 Change C189 from 100p to 470p for noise

Reserve C189 for PLT_RST# 0423 place C189 close to U34.AN6



0522 Add R152-R156 for non-use HDA signals D.G p.190



0517 Delete R500/R504 and add T17

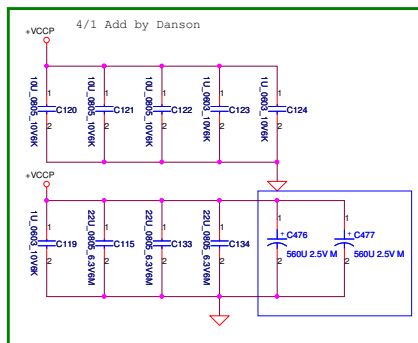
G41 not support C3/C4
D.G recommend SLB# NC,
DPRSTP# pull up 49.9 ohm to V_FSB_VTT



0517 Delete R518 and VGATE off page

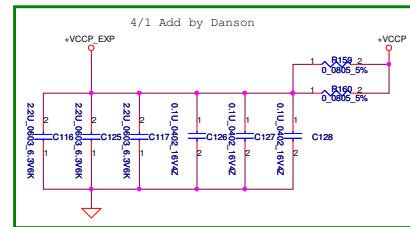


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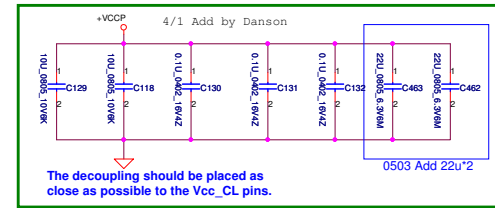
17.984A

1.345A



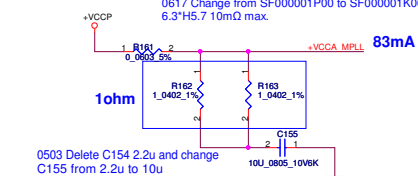
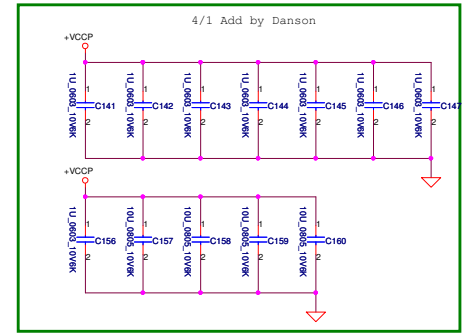
0.914A

4.06A



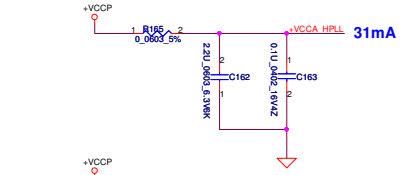
The decoupling should be placed as close as possible to the Vcc_CL pins.

0503 Add 22u*2

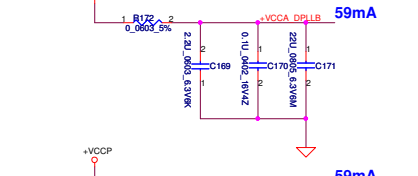


83mA

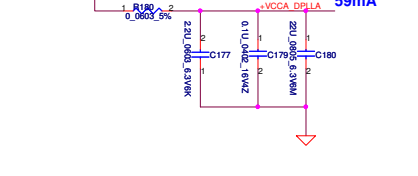
0503 Delete C154 2.2u and change C155 from 2.2u to 10u



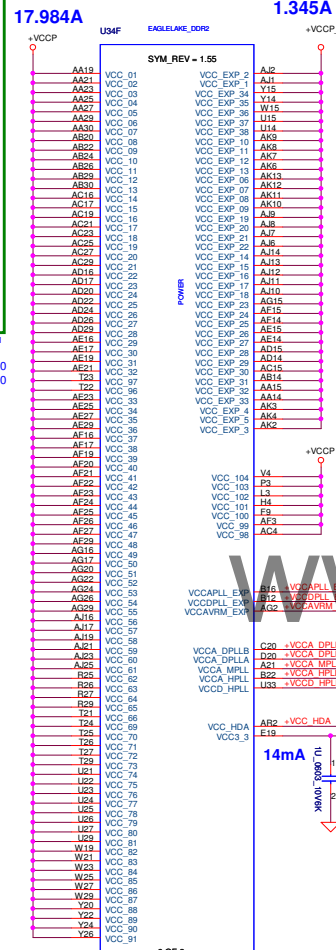
31mA



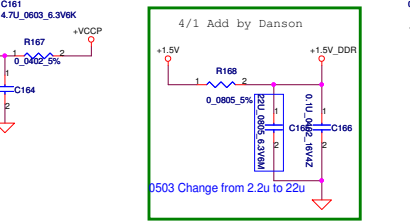
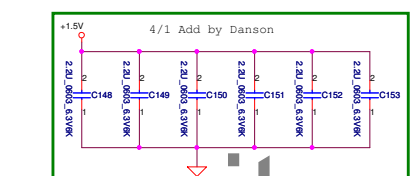
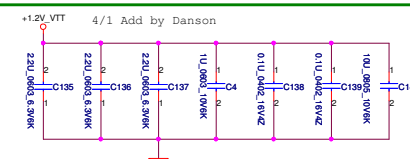
59mA



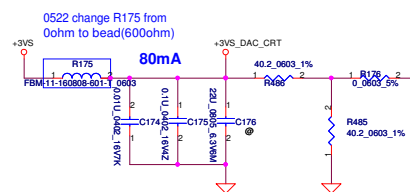
59mA



Change GMCH P/N to SA000042U10 for T88



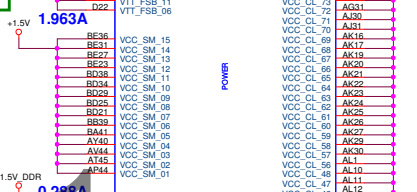
0503 Change from 2.2u to 22u



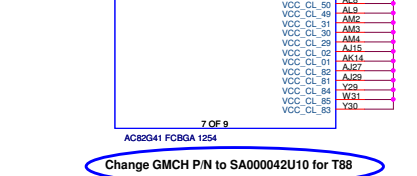
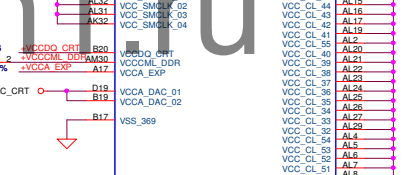
0522 change R175 from 0ohm to bead(600ohm)



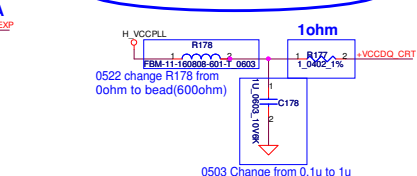
0503 Delete C181 0.1u



1.963A



Change GMCH P/N to SA000042U10 for T88

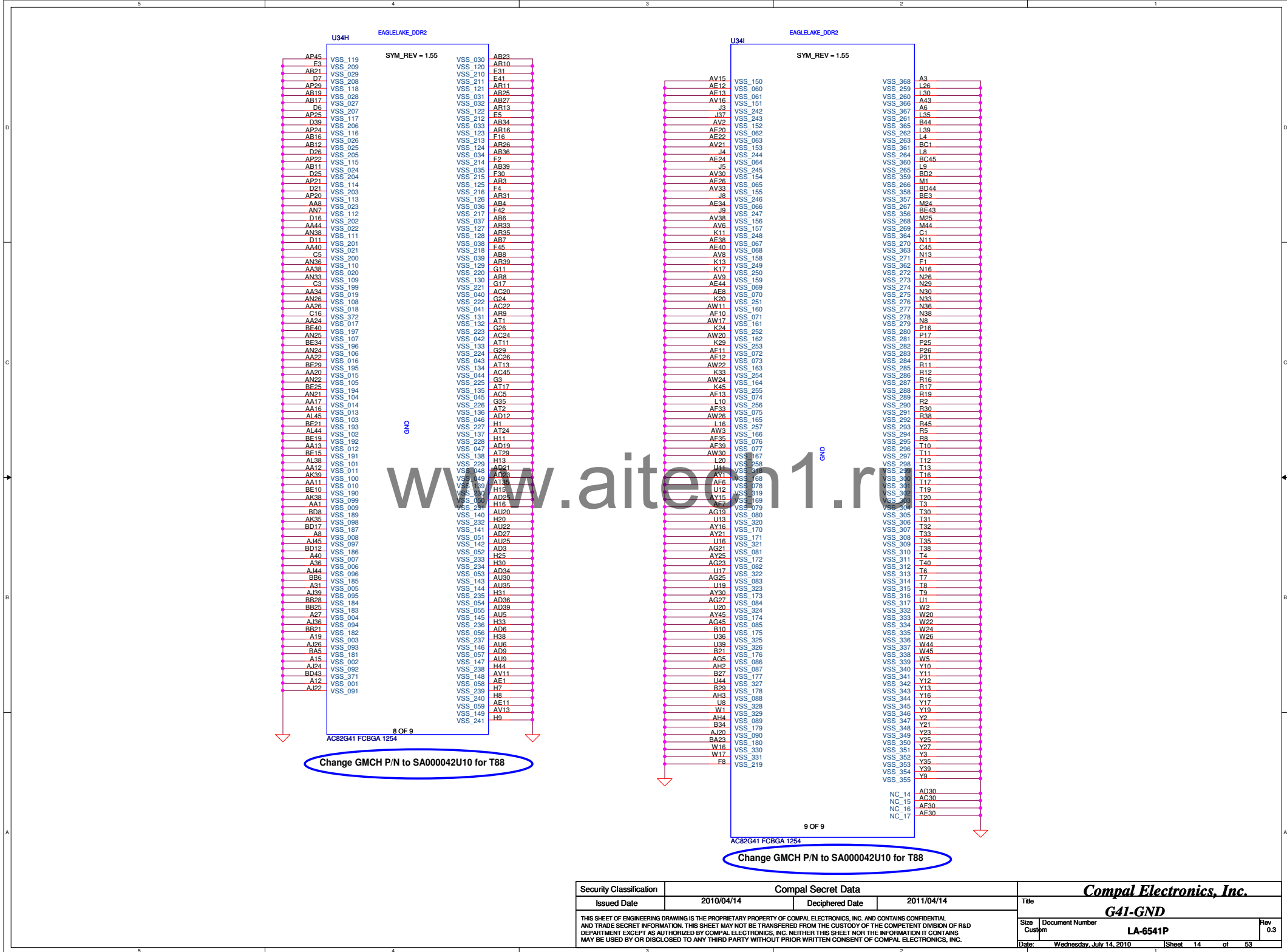


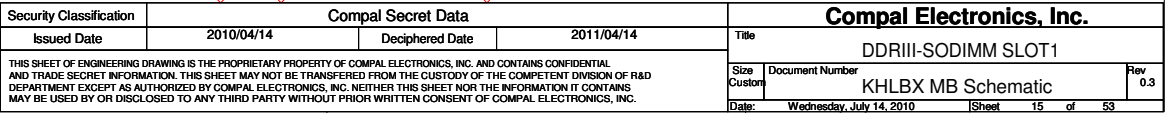
0522 change R178 from 0ohm to bead(600ohm)

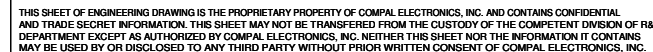


0503 Change from 0.1u to 1u

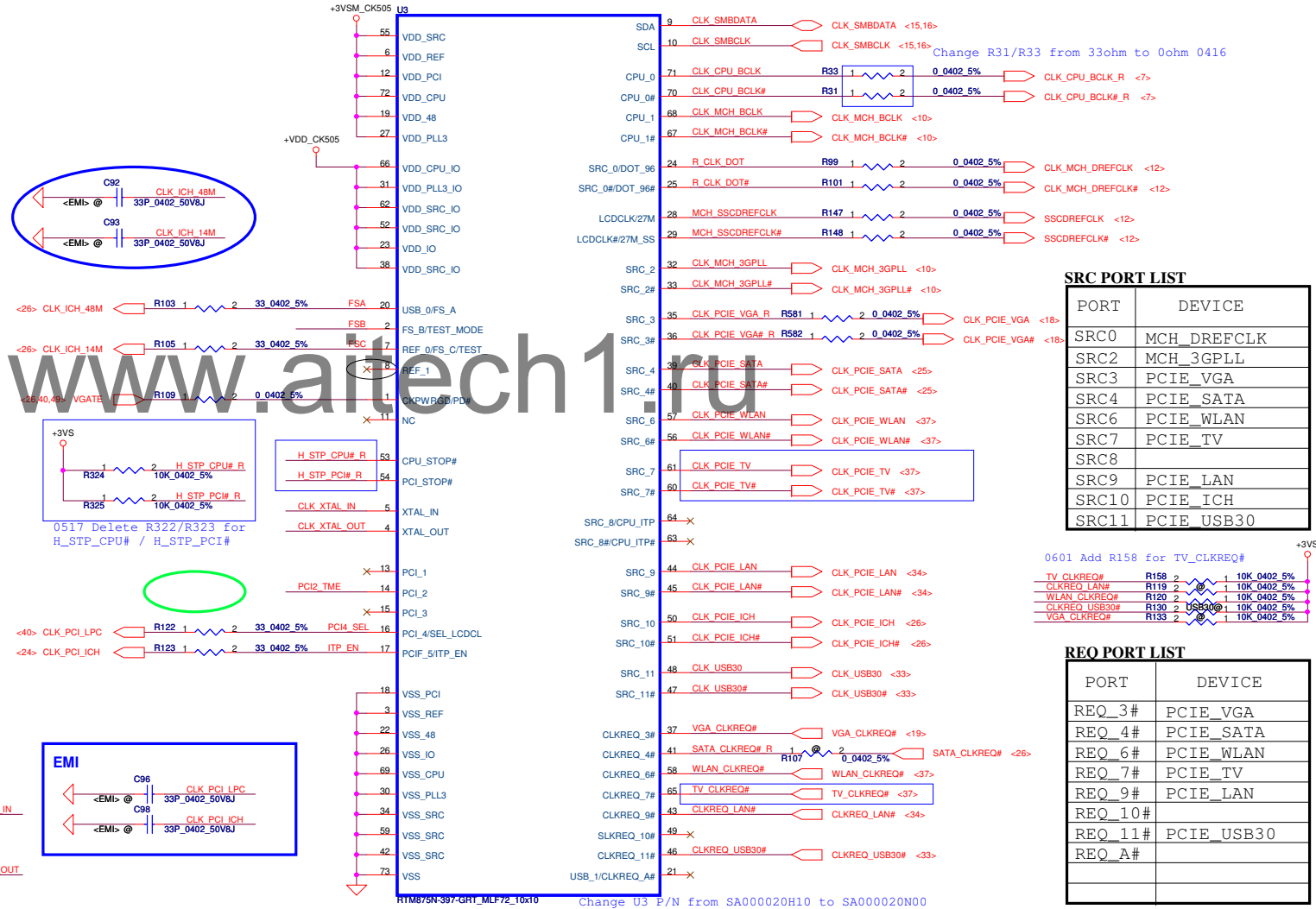
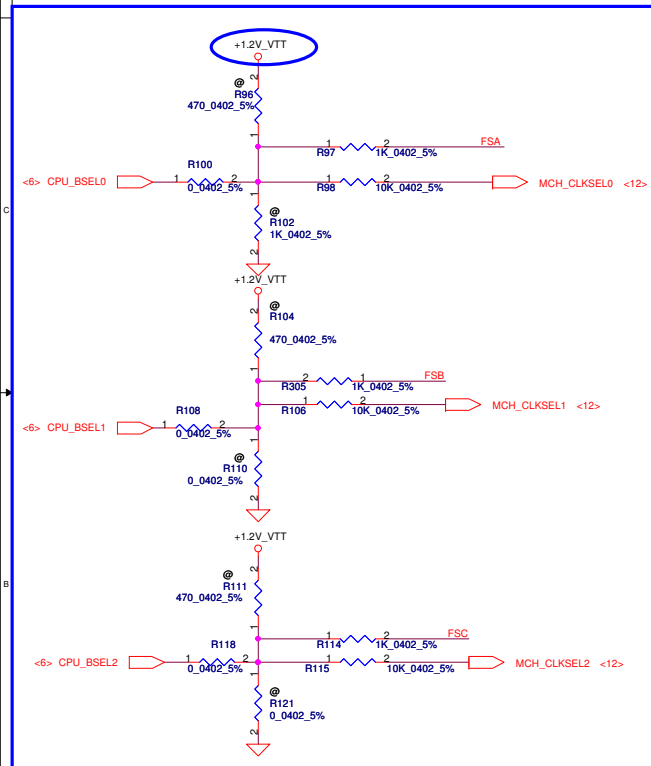
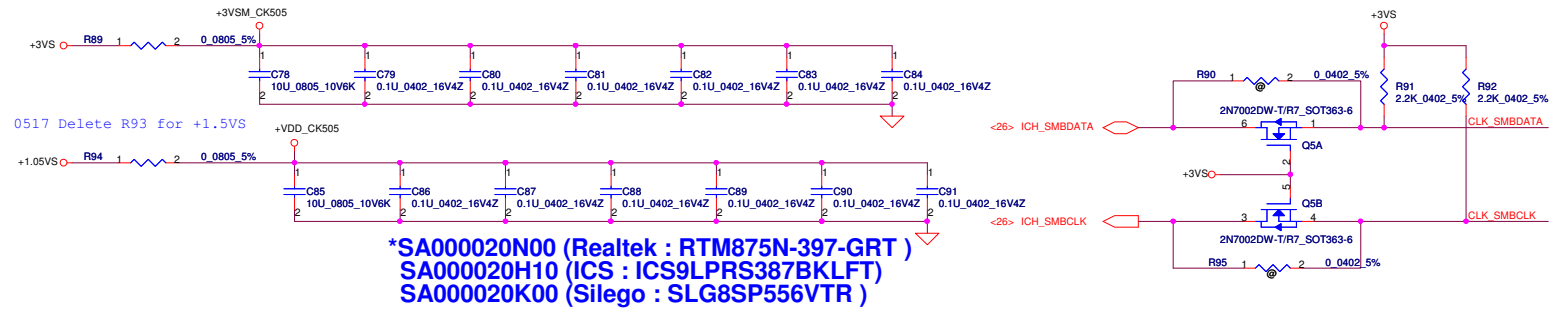
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FSC	FSB	FSA	CPU	SRC	PCI	REF	DOT_96	USB
CLKSEL2	CLKSEL1	CLKSEL0	MHz	MHz	MHz	MHz	MHz	MHz
0	0	0	266	100	33.3	14.318	96.0	48.0
0	0	1	133	100	33.3	14.318	96.0	48.0
0	1	0	200	100	33.3	14.318	96.0	48.0
0	1	1	166	100	33.3	14.318	96.0	48.0
1	0	0	333	100	33.3	14.318	96.0	48.0
1	0	1	100	100	33.3	14.318	96.0	48.0
1	1	0	400	100	33.3	14.318	96.0	48.0
1	1	1	Reserved					



SRC PORT LIST

PORT	DEVICE
SRC0	MCH_DREFCLK
SRC2	MCH_3GPLL
SRC3	PCIE_VGA
SRC4	PCIE_SATA
SRC6	PCIE_WLAN
SRC7	PCIE_TV
SRC9	PCIE_LAN
SRC10	PCIE_ICH
SRC11	PCIE_USB30

REQ PORT LIST

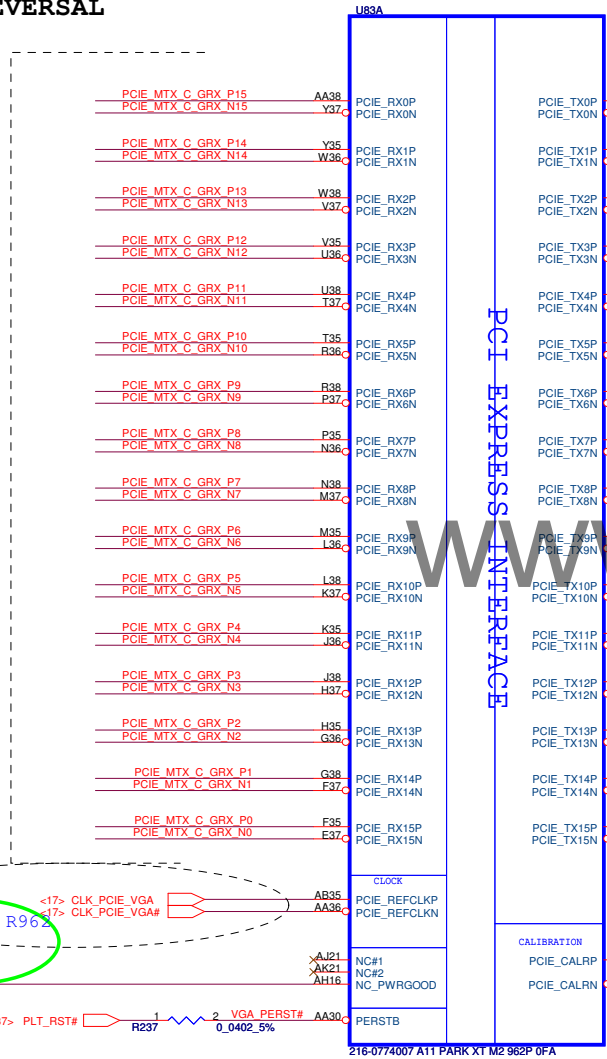
PORT	DEVICE
REQ_3#	PCIE_VGA
REQ_4#	PCIE_SATA
REQ_6#	PCIE_WLAN
REQ_7#	PCIE_TV
REQ_9#	PCIE_LAN
REQ_10#	
REQ_11#	PCIE_USB30
REQ_A#	

For ITP_EN, 0 = SRC8/SRC8#; 1 = ITP/ITP#
For PCI2_SEL, 0 = Pin24/25 : DOT96 / DOT96#
Pin28/29 : LCDCLK / LCDCLK#
1 = Pin24/25 : SRC_0 / SRC_0#
Pin28/29 : 27M/27M_SS

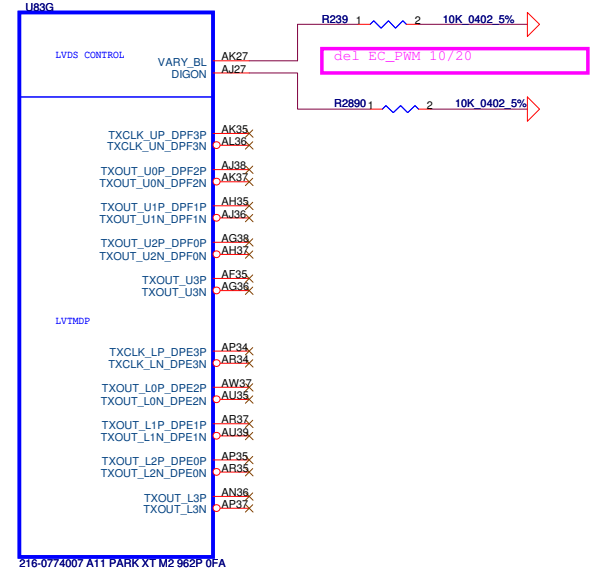
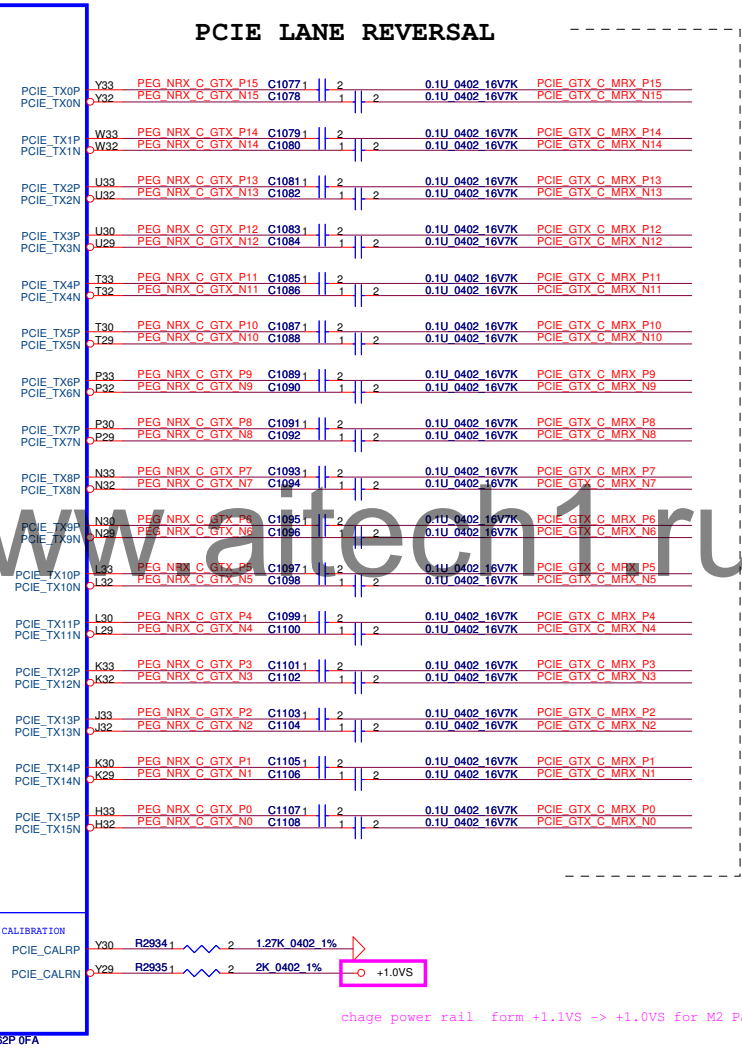
For PCI2_TME, 0 = overclocking of CPU and SRC allowed (RTM only) 1 = overclocking of CPU and SRC not allowed

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Issued Date	2010/04/14	Deciphered Date	2011/04/14	Clock Generator CK505	
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				LA-6541P	Rev 0.3
				Date: Wednesday, July 14, 2010	Sheet 17 of 53

PCIE LANE REVERSAL



PCIE LANE REVERSAL



M96 P/N : SA00002UQ50 (S IC 216-0729042-00 A13 M96 FCBGA962 0FA)
M92 P/N : SA00002YX10 (S IC 216-0728014 A12 M92-M2 XT FCBGA 0FA)

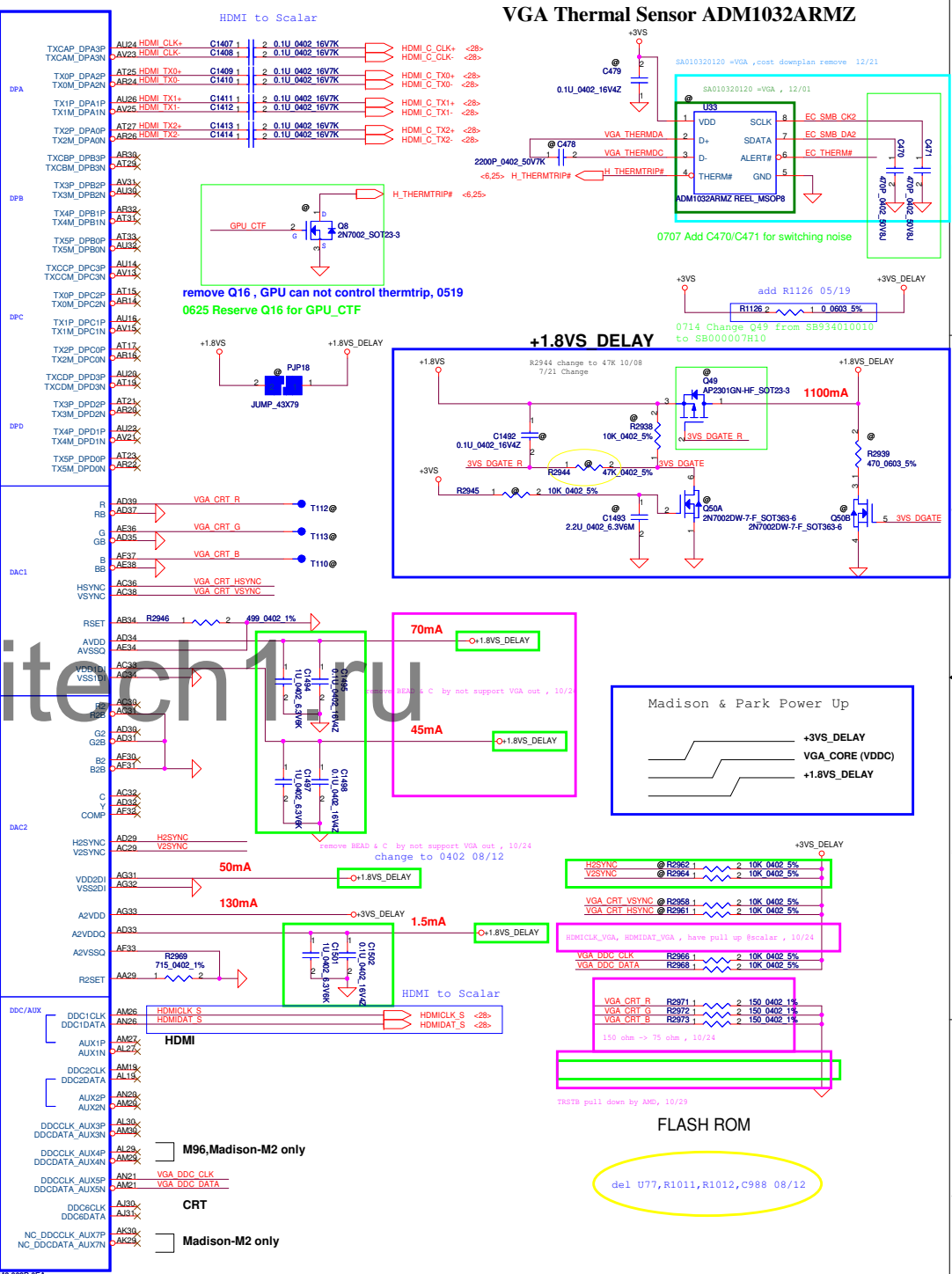
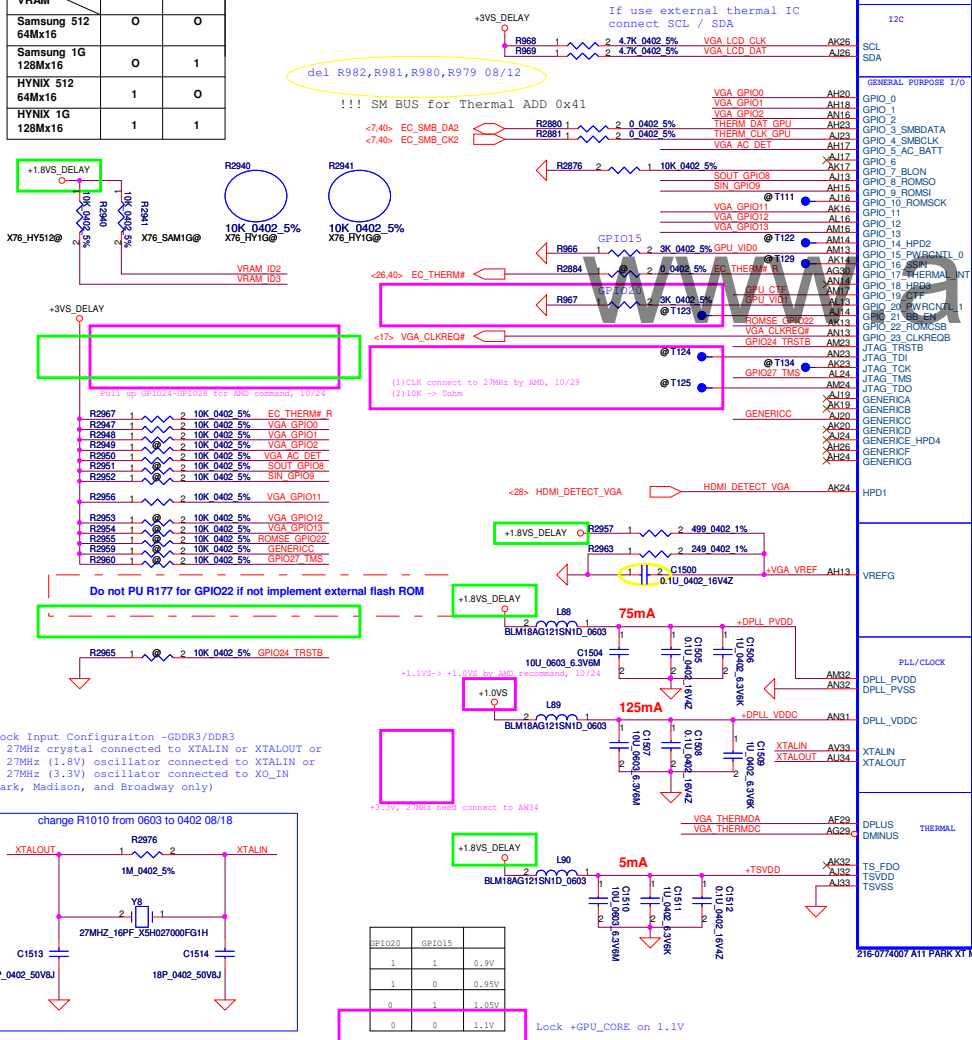
MADISON P/N:SA00003M300 (S IC 216-0772000 MADISON PRO FCBGA 0FA)
PARK P/N:SA00003MC00 (S IC 216-0774007 A11 PARK PRO M2 0FA)

SA00003MC10->SA00003MC50 for T88 material 11/18

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2010/04/14	Deciphered Date	2010/07/14	PARK PCIE / LVDS	
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				Date	Wednesday, July 14, 2010
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Strap Name		Pin Straps Description	Default
TX_PWRS_ENB	GPIO0	Transmitter Power Saving Enable 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)	0
TX_DEEMPH_EN	GPIO1	PCI Express Transmitter De-emphasis Enable 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled (Default setting for desktop)	0
BIF_GEN2_EN	GPIO2	0: Advertises the PCI-E device as 2.5 GT/s capable at power-on 1: Advertises the PCI-E device as 5.0 GT/s capable at power-on 5.0 GT/s capability will be controlled by software	0
STRAP_BIF_CLK_PM_EN	GPIO22	Enable CLKREQ# Power Management 0: CLKREQ# power management capability is disabled 1: CLKREQ# power management capability is enabled	0
CONFIG[2] CONFIG[1] CONFIG[0]	GPIO13 GPIO12 GPIO11	GPIO13,12,11 (config 2,1,0) : a) If BIOS_ROM_EN = 1, then Config[2:0] defines the ROM type. b) If BIOS_ROM_EN = 0, then Config[2:0] defines the primary memory aperture size.	001
BIOS_ROM_EN	GPIO22	Enable external BIOS ROM device 0: Disable, 1: Enable	0
AUD[1] AUD[0]	HSYNC VSYNC	00: No audio function; 10: Audio for DisplayPort only; 01: Audio for DisplayPort and HDMI if adapter is detected; 11: Audio for both DisplayPort and HDMI	11
CCBPASS	GENERICC		0
SMS_EN_HARD	H2VSYNC		0
VIP_DEVICE_STRAP_DIS	V2VSYNC	If VIP_DEVICE_STRAP_EN is set to ?? then this pin is used to sense whether a VIP slave device is connected to the VIP Host interface. If VIP_DEVICE_STRAP_EN is set to ?? then this pin is used as a strap at all (i.e. its value during reset is unimportant), and it can be used as a regular GPIO	0

Location	VRAM_ID3	VRAM_ID2
VRAM		
Samsung 512 64Mx16	0	0
Samsung 1G 128Mx16	0	1
HYNIX 512 64Mx16	1	0
HYNIX 1G 128Mx16	1	1



Security Classification	Compal Secret Data	Deciphered Date	2010/07/14
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Title		PARK Strape/DP/HDMI/CRT	
Size C	Document Number	LA-6541P	
Date:	Wednesday, July 14, 2010	Sheet	19 of 53

For DDR3 , MVDDQ=1.5V

+1.5VS

C1572

1U 0402 6.3V6K

C1571

1U 0402 6.3V6K

C1570

1U 0402 6.3V6K

C1569

1U 0402 6.3V6K

C1568

1U 0402 6.3V6K

C1567

1U 0402 6.3V6K

C1566

1U 0402 6.3V6K

C1565

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C1564

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C1563

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C1562

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C1514

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C1512

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C1511

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C1510

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C1509

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C1508

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C1507

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C1506

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C1505

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C1504

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C1503

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C1502

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C1501

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C1500

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C1434

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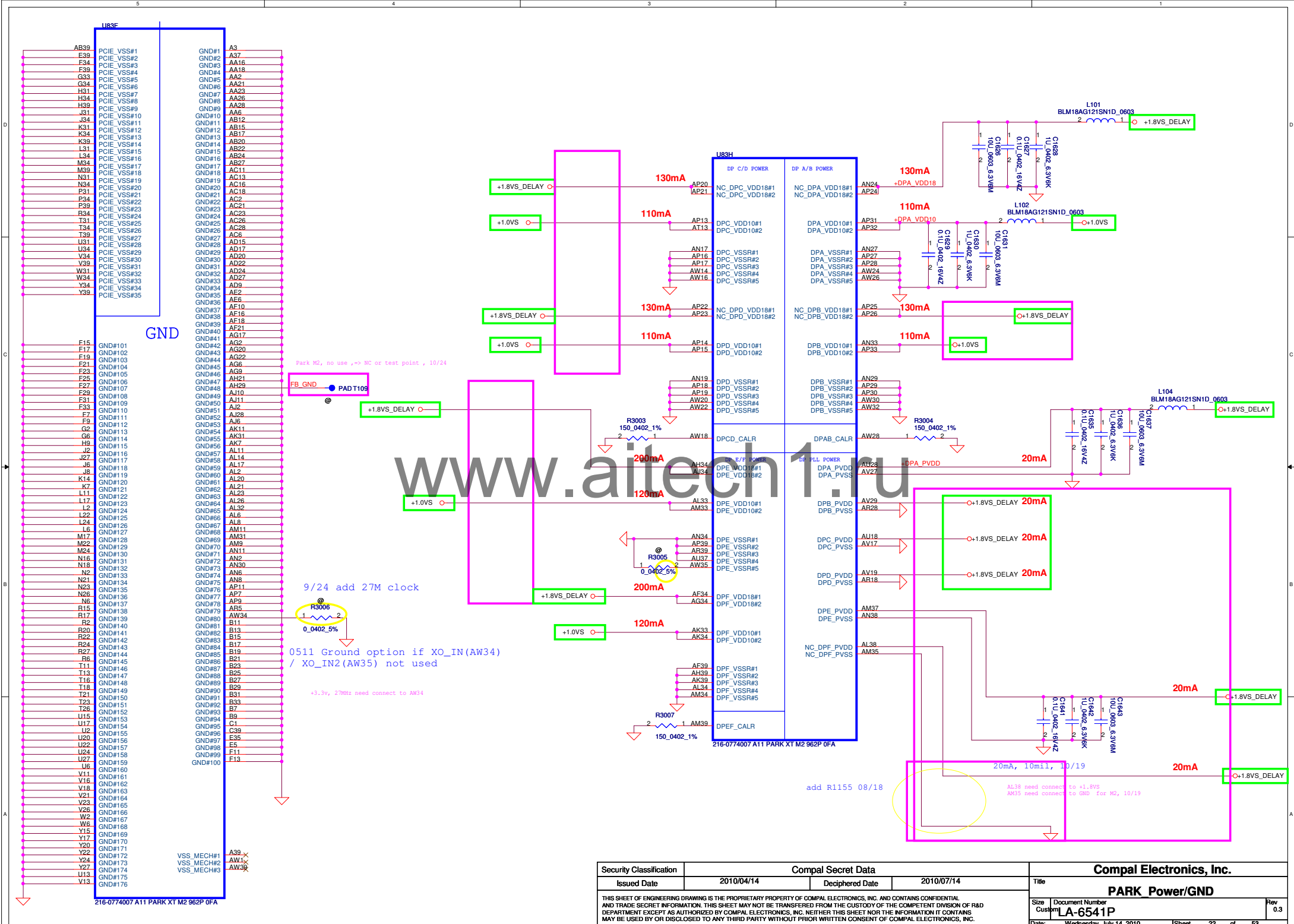
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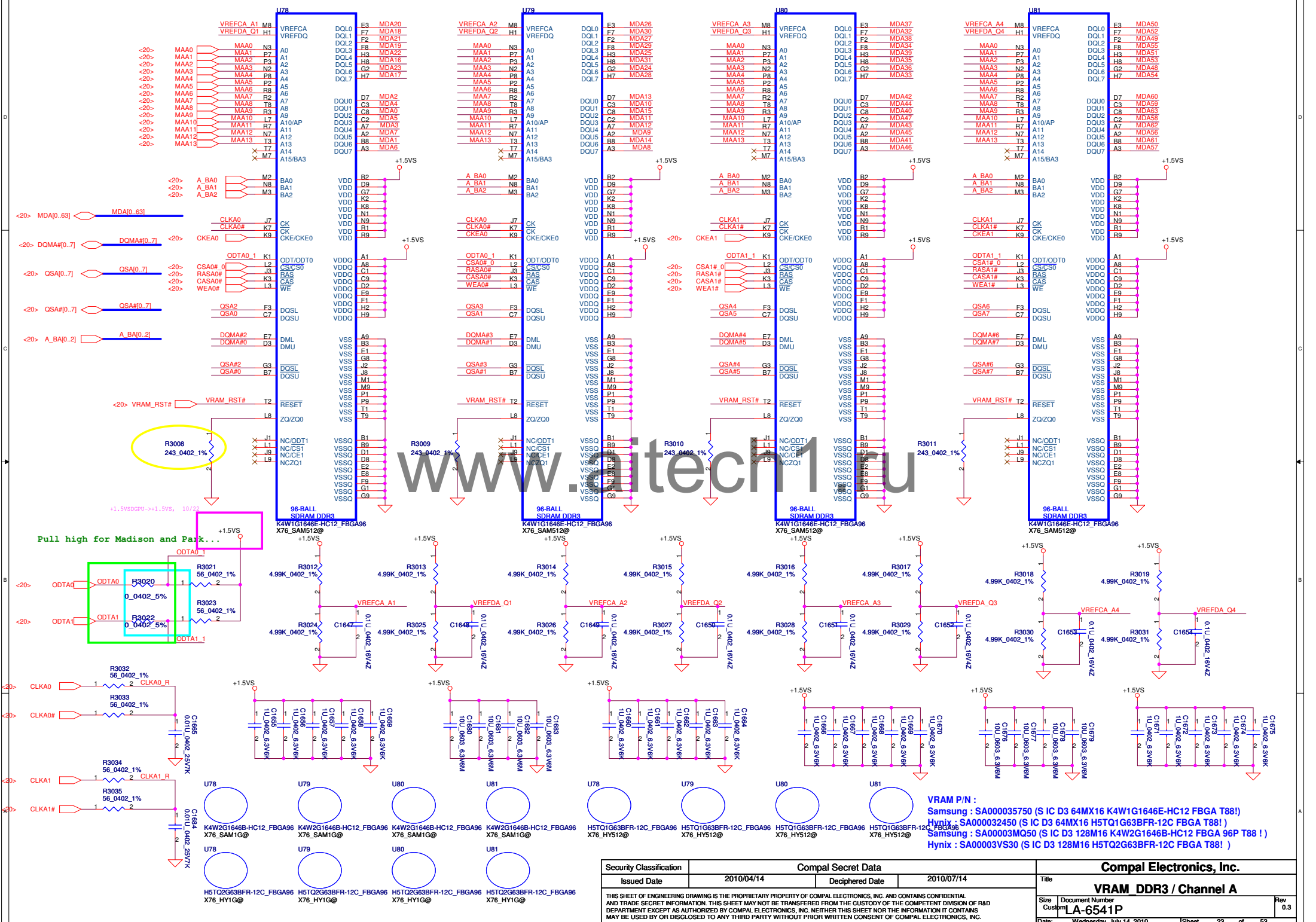
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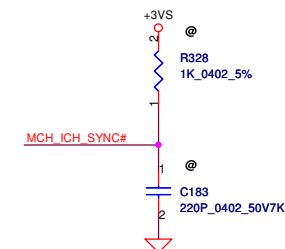
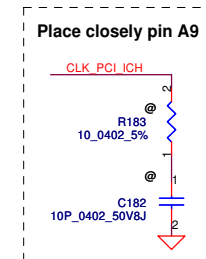
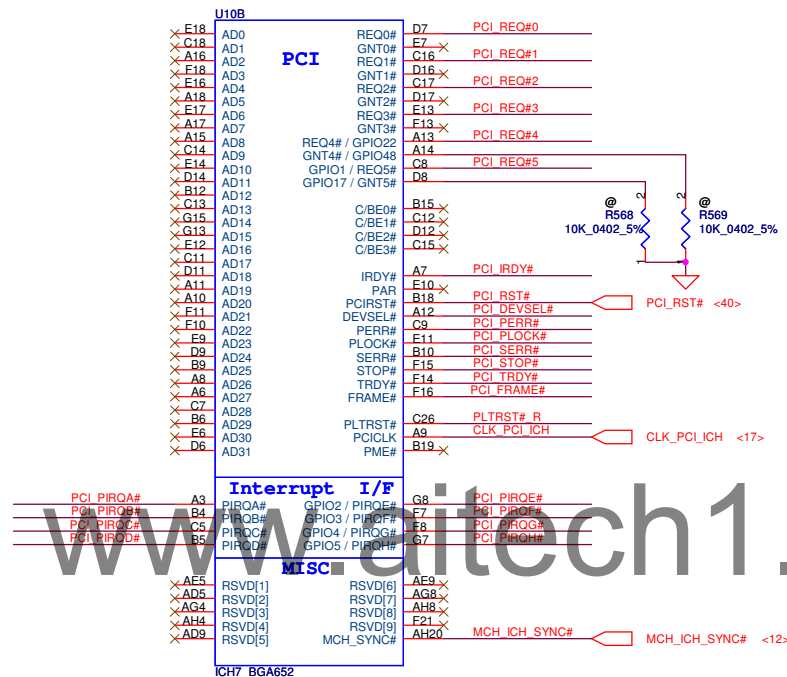
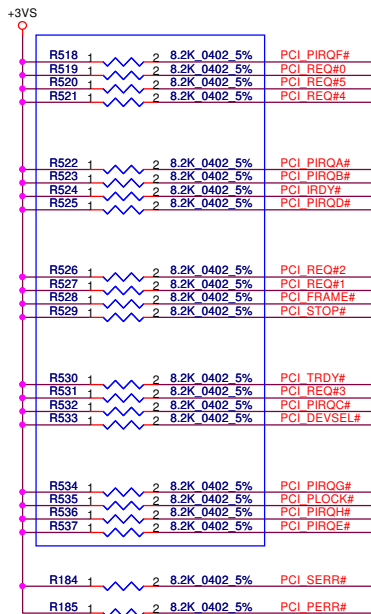
C1431



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				Date	Wednesday, July 14, 2010
				Sheet	22 of 53

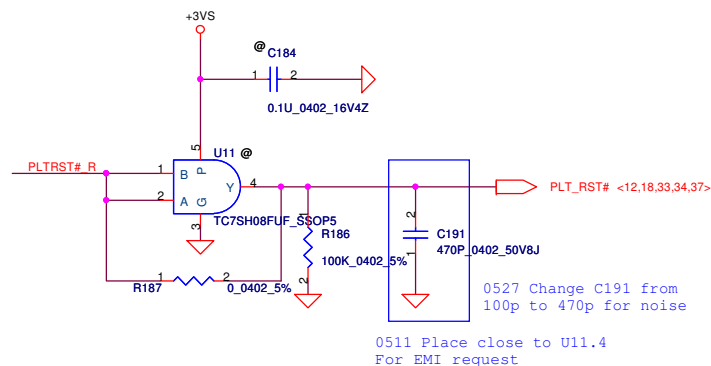


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						Size		Document Number		Rev	
						Custom		LA-6541P		0.3	
						Date:		Wednesday, July 14, 2010		Sheet 23 of 53	



Change ICH7 P/N to SA000042V10 for T88

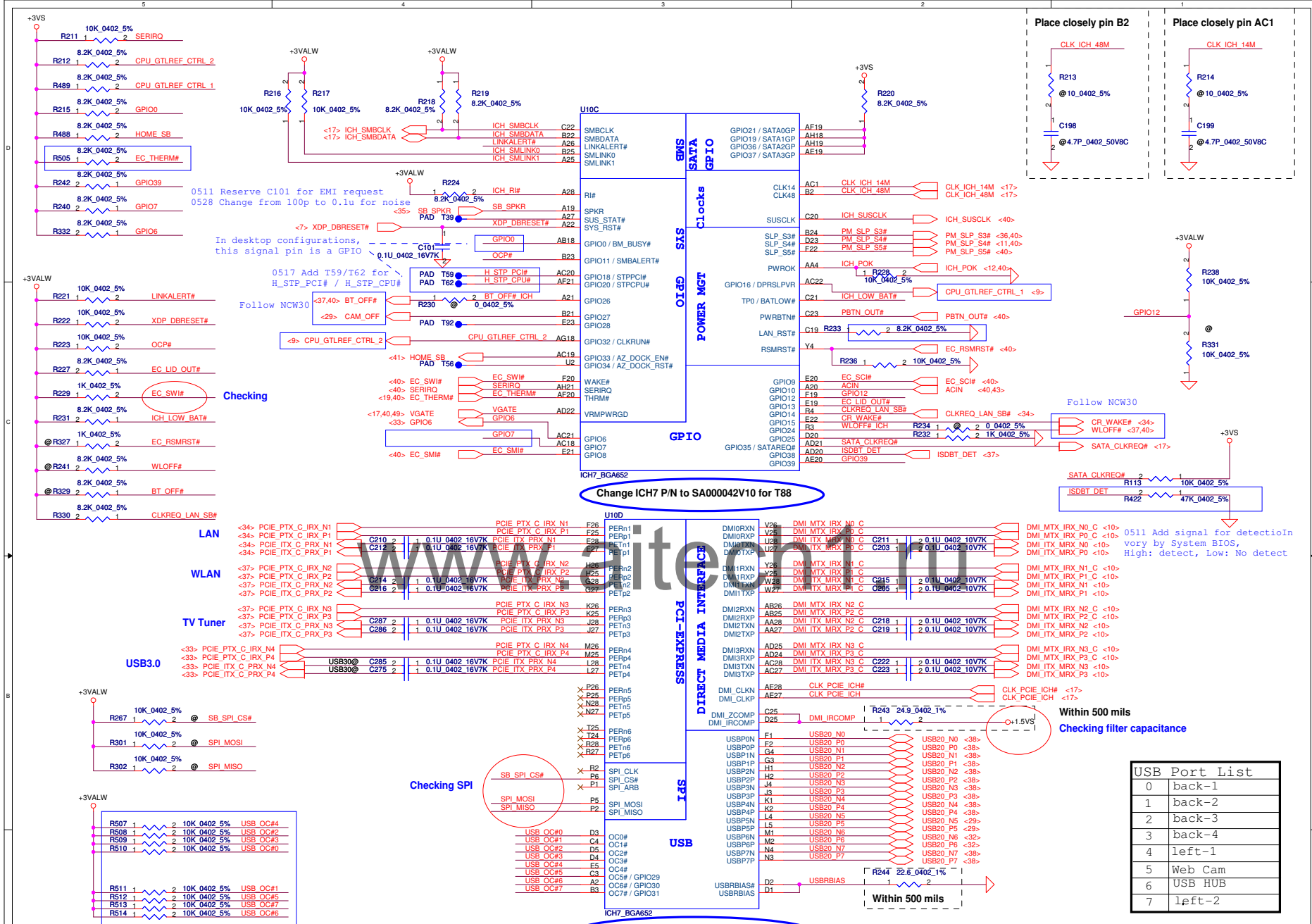
GPIO17	GPIO48	Boot BIOS
0	1	SPI
1	0	PCI
1	1	LPC



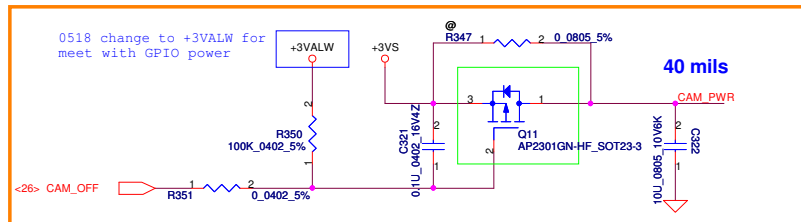
0511 Place close to U11.4
For EMI request

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Size	Custom	Document Number	LA-6541P	Rev	0.3
Date:	Wednesday, July 14, 2010	Sheet	24	of	53

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						Size	Document Number	Rev
						Custom	LA-6541P	0.3
Date:		Wednesday, July 14, 2010		Sheet	25	of 53		

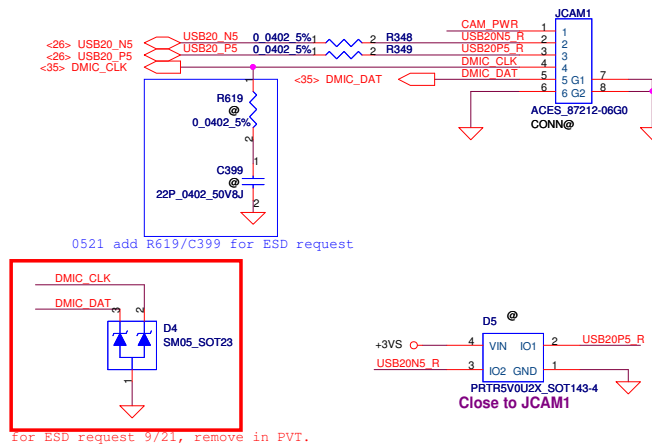


WebCam+Digital Mic

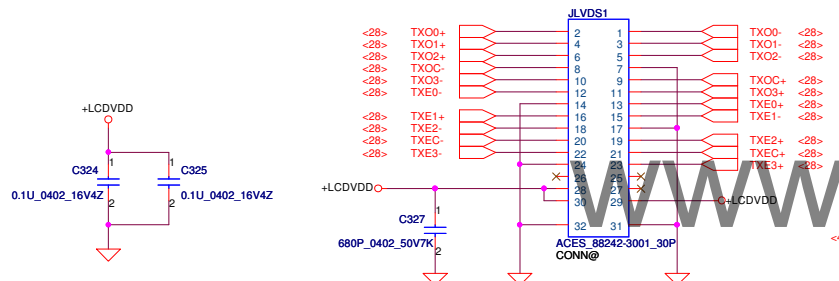


Pre-MP for WebCam off control by BIOS.

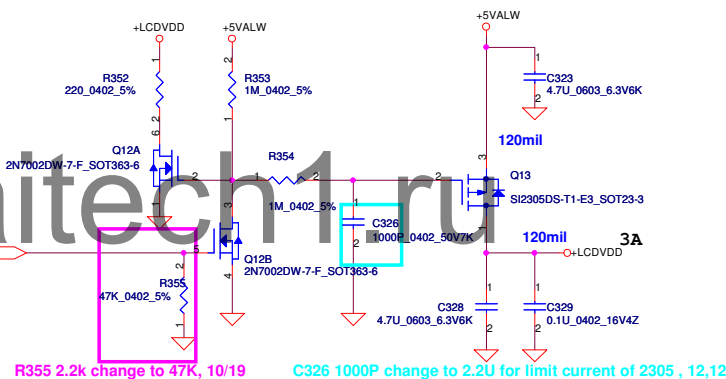
0714 Change Q11 from SB934010010 to SB000007H10



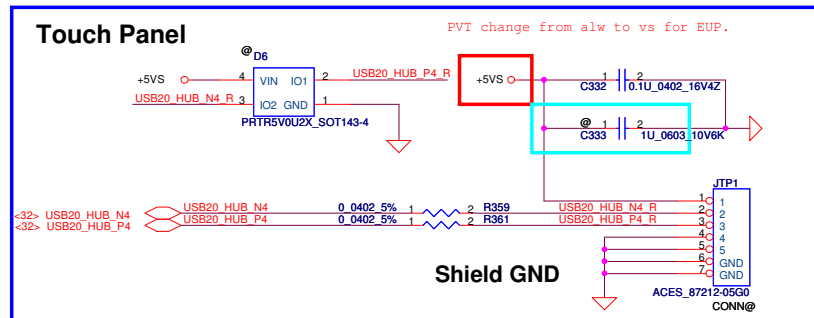
LVDS CONN



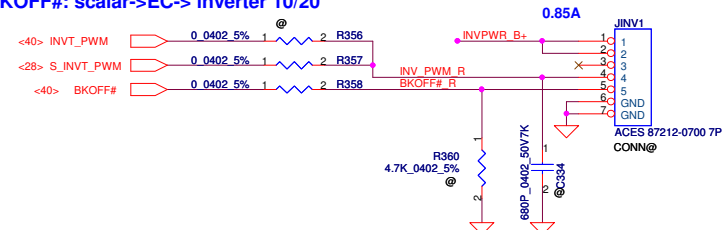
LVDS POWER



Touch Panel

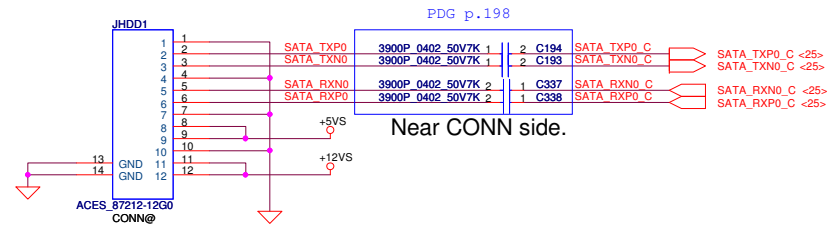
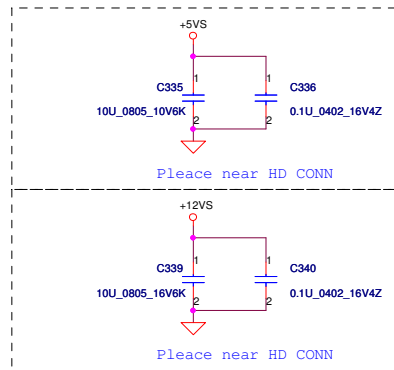


ENVDD: scalar->EC-> inverter
INVT_PWM: scalar-> inverter
BKOFF#: scalar->EC-> inverter 10/20



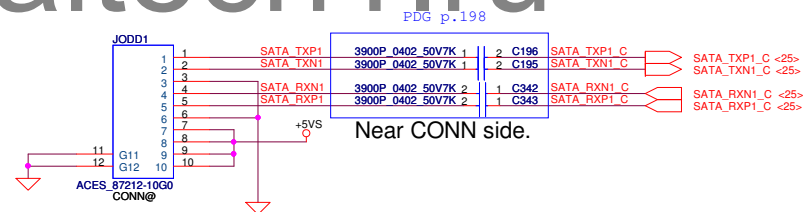
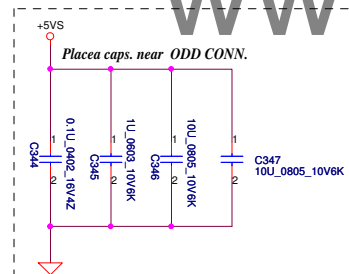
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Issued Date	2010/04/14	Deciphered Date	2011/04/14	Title		
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				Size	Document Number	Rev
				Custom	LA-6541P	0.3
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HDD : 5V X2 , 12 V X2



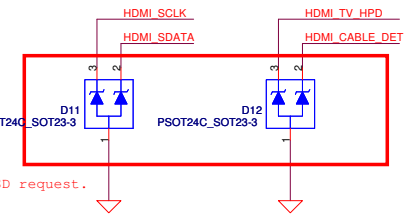
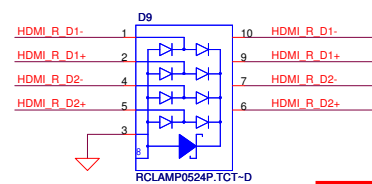
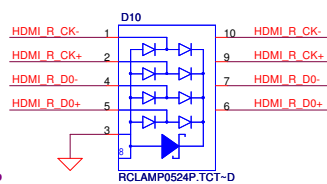
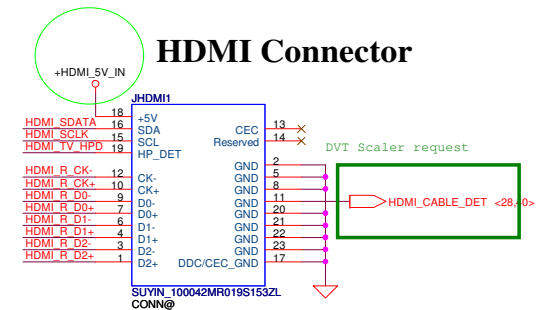
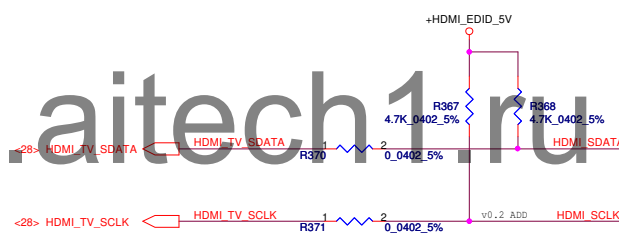
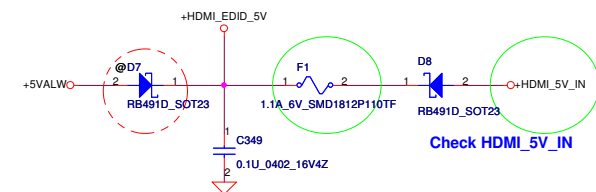
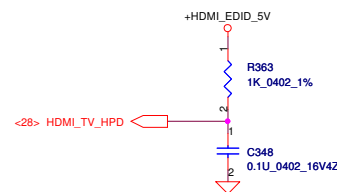
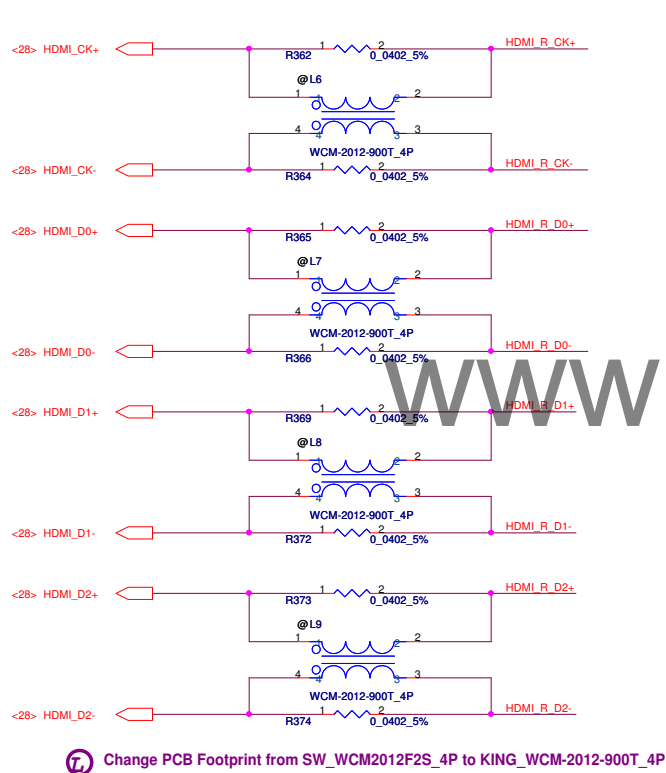
ODD : 5V X2

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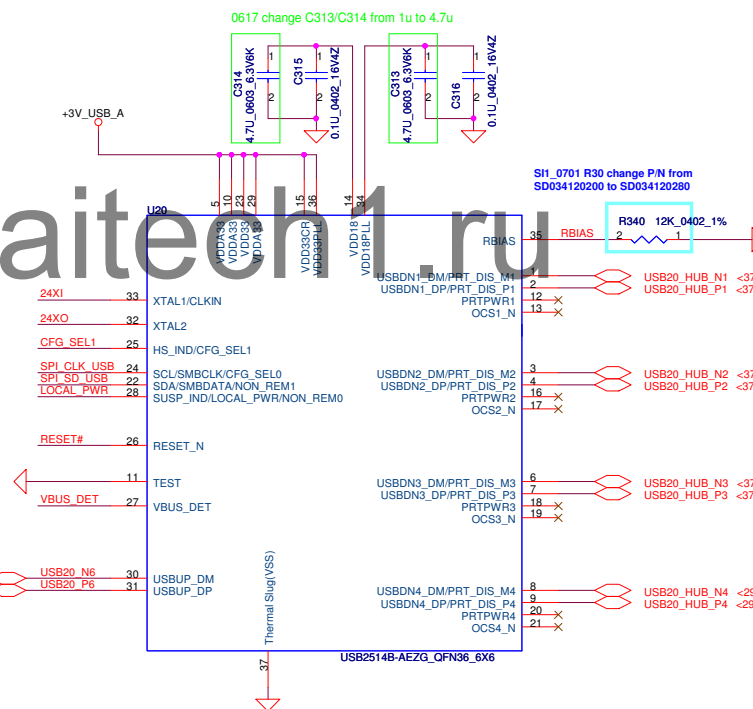
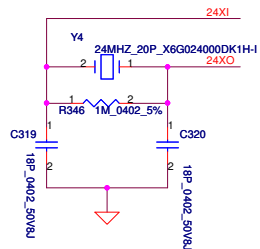
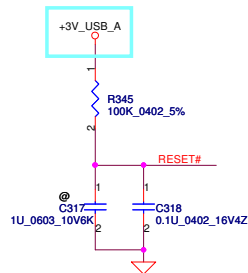
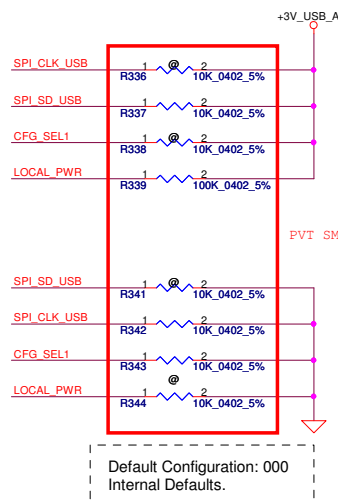
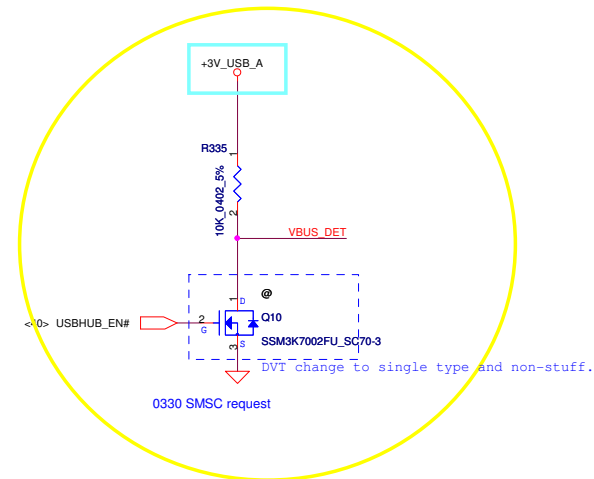
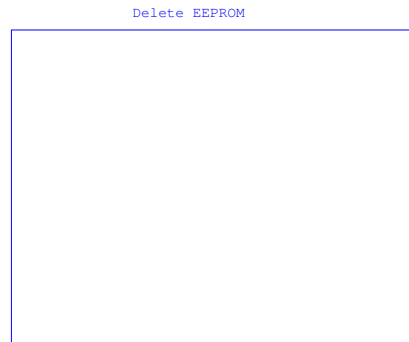
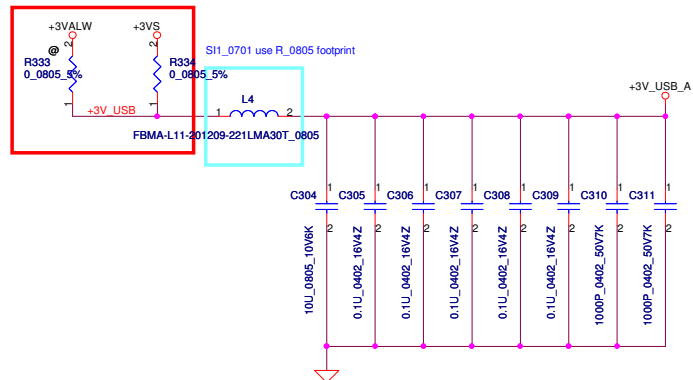
Security Classification		Compal Secret Data		Compal Electronics, Inc. HDD/CDROM		
Issued Date	2010/04/14	Deciphered Date	2011/04/14	Title		
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External

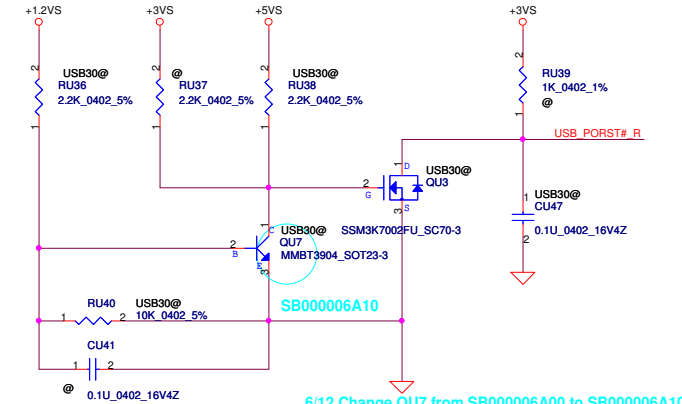


Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2010/04/14	Deciphered Date	2011/04/14	Title	
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Size	Document Number	Rev		0.3	
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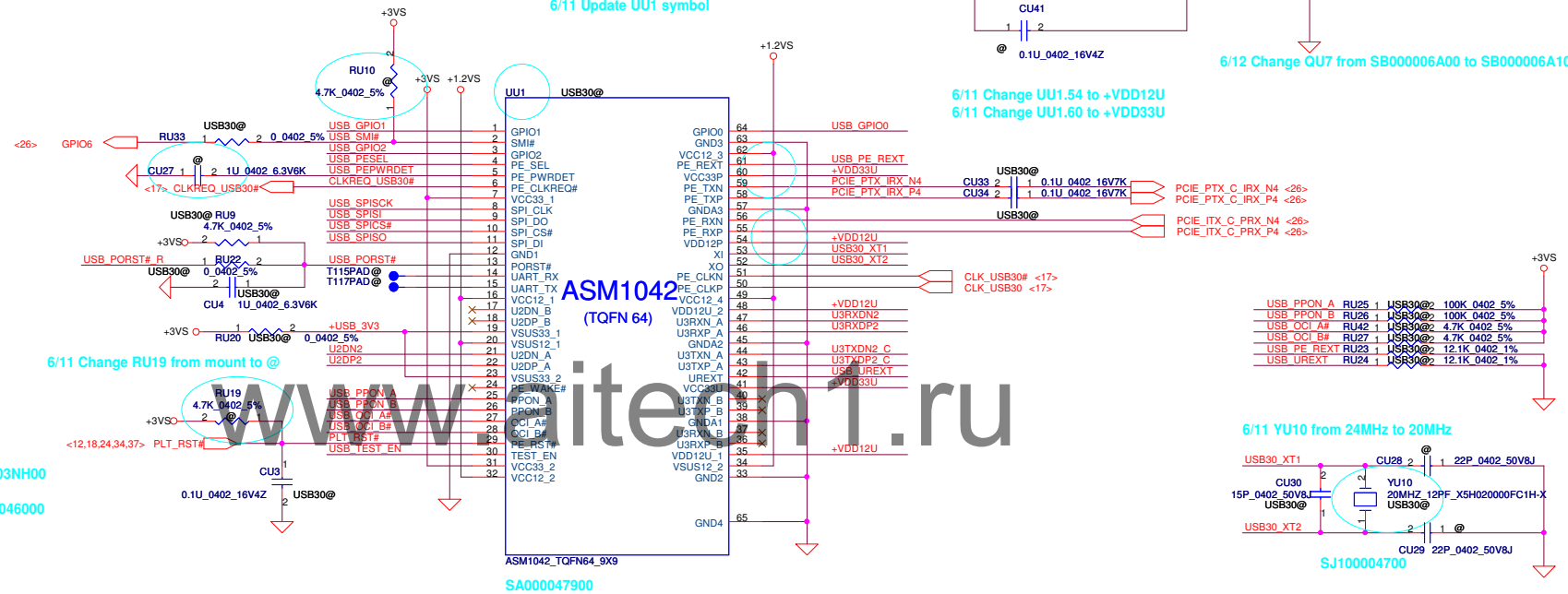
PVT change from alw to vs for EUP and function lost issue.



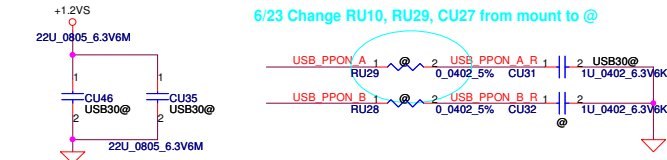
HUB Port List	
0	BT
1	TV Tuner
2	B-CAS
3	TS



6/11 Update UU1 symbol



6/23 Change RU10, RU29, CU27 from mount to @

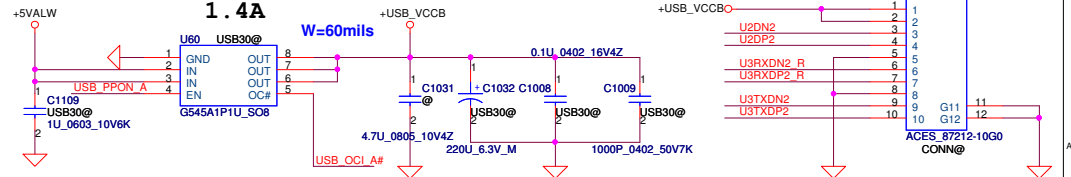
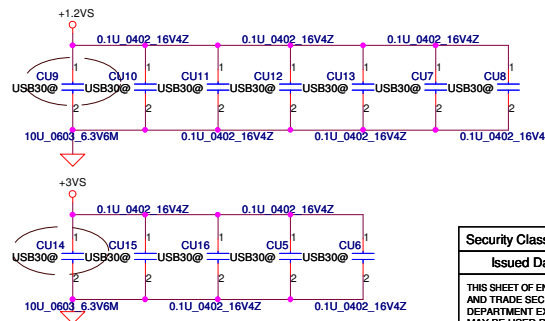


must to close to JUSB30

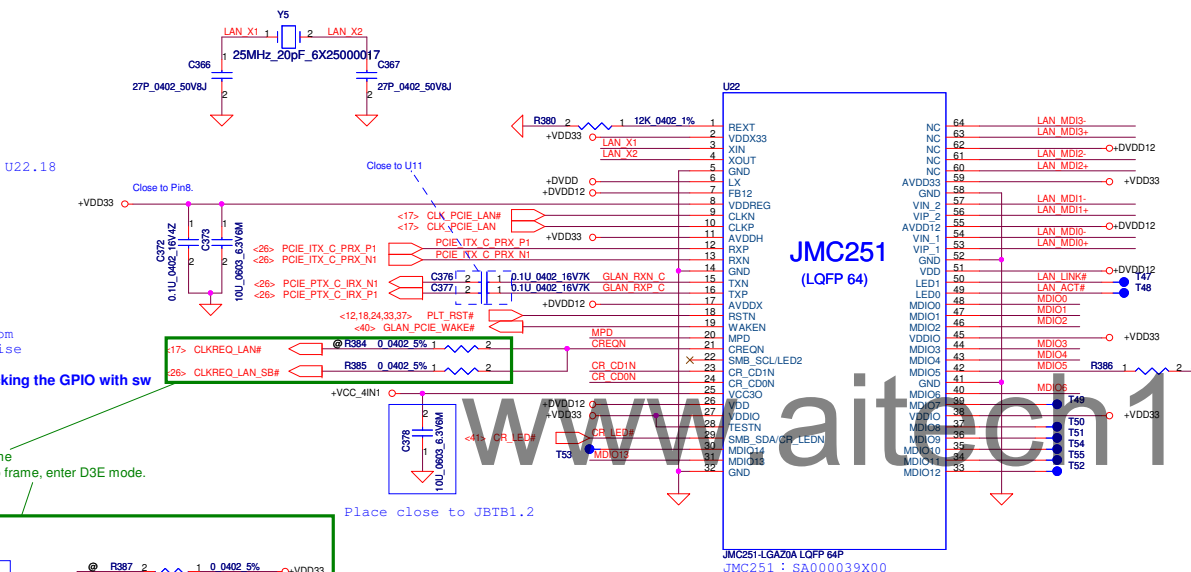
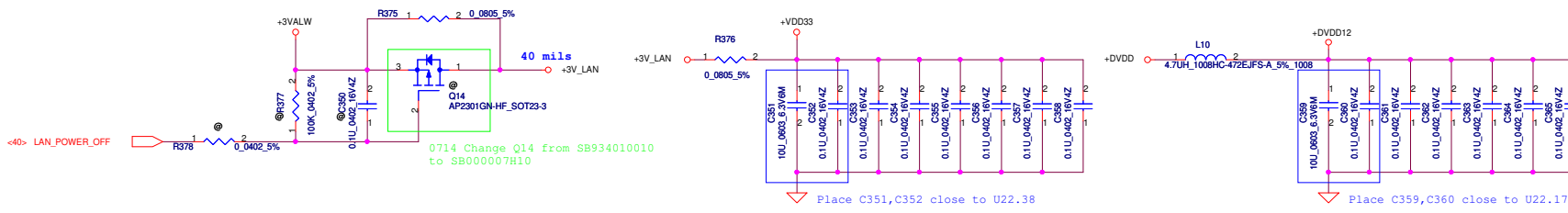
USB_PEPWRDET		
	RU6	RU7
S1	Mount	@
S3	@	Mount

U3RXDN2	USB30@	CU3	2	1	0.1U	0402	16V7K	U3RXDN2 R
U3RXDP2	USB30@	CU4	2	1	0.1U	0402	16V7K	U3RXDP2 R
U3TXDN2 C	USB30@	CU4	4	2	1	0.1U	0402	16V7K
U3TXDP2 C	USB30@	CU5	2	1	0.1U	0402	16V7K	U3TXDP2

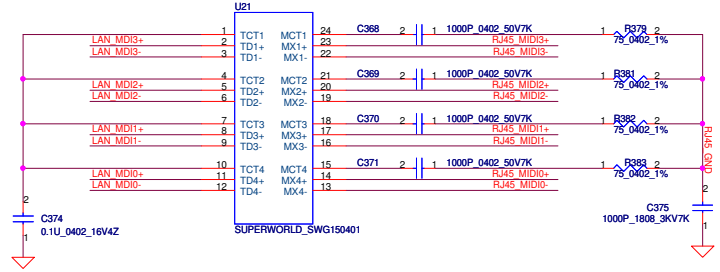
0713 Change U60 to G545A1P1U



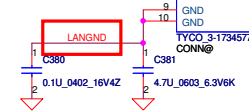
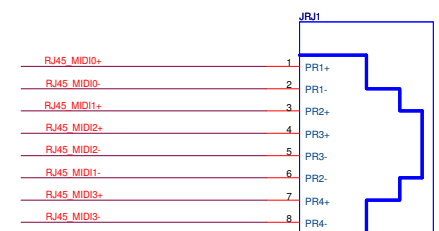
Security Classification		Compal Secret Data		Compal Electronics, Inc.		
Issued Date	2010/03/04	Deciphered Date	2011/03/04	Title PCIe-USB3.0		
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					PAQ10 LA6461P M/B	0.3
				Date:	Wednesday, July 14, 2010	Sheet 33 of 53



10/100 and Giga Transformer Co lay

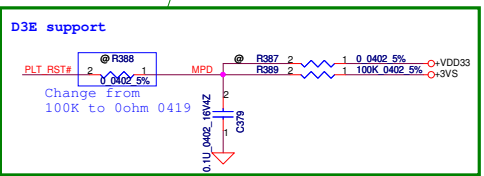
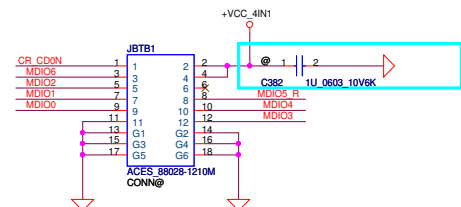


LAN Conn.

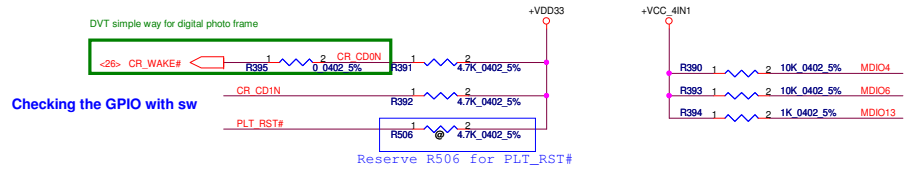


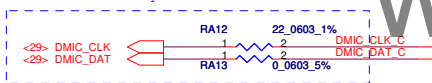
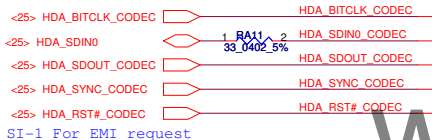
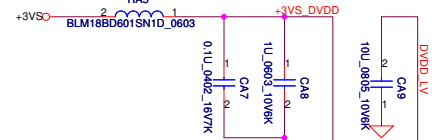
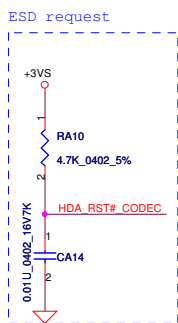
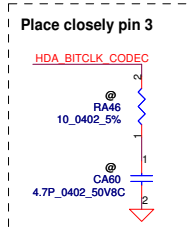
Card Reader Connector

BTB connector



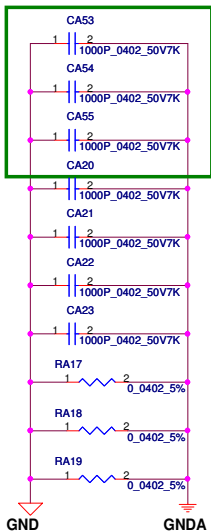
R387	R389	R388	C379	Function
0	NC	NC	NC	Disable D3E
NC	NC	0	NC	Enable D3E(1)
NC	100K	NC	0.1u	Enable D3E(2)



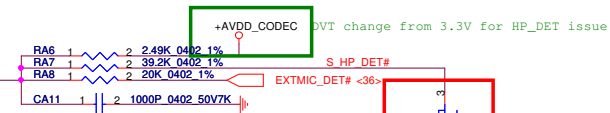
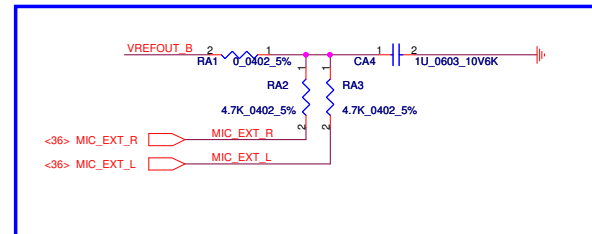
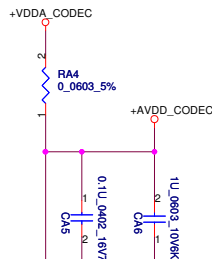


Camera MIC

DVT add three more GNDA caps for ESD request



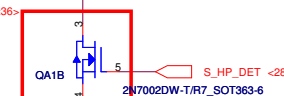
(4.75V(4.56~4.94V)) 300mA



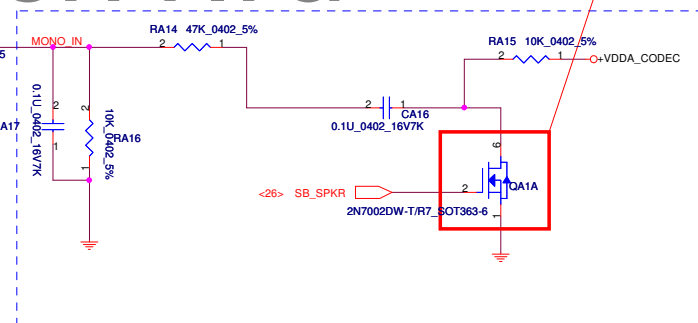
HP Jack

Jack MIC

Internal SPKR.



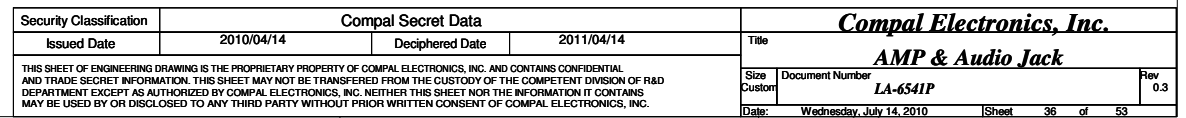
PVT change to dual die.



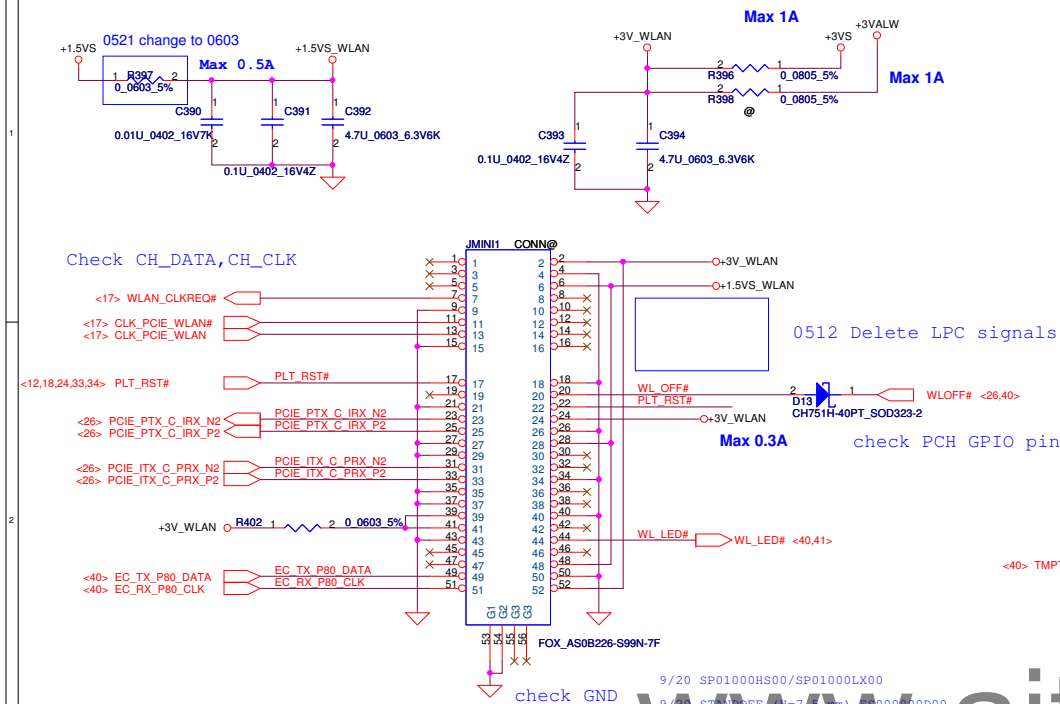
090212 For PC Beep Noise

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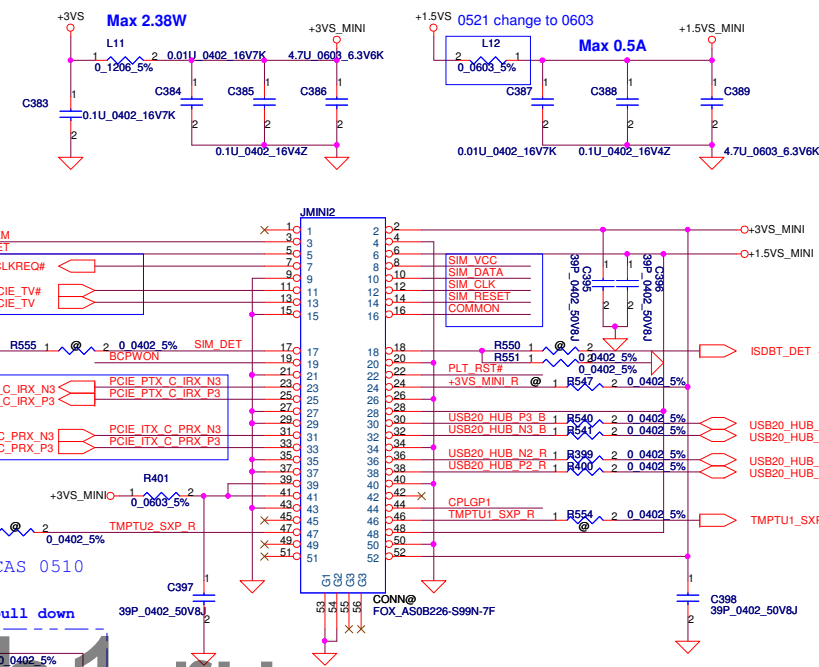
GAIN0	GAIN1	Av (inv)
0	0	10dB
0	1	12dB
1	0	15.6dB
1	1	21.6dB



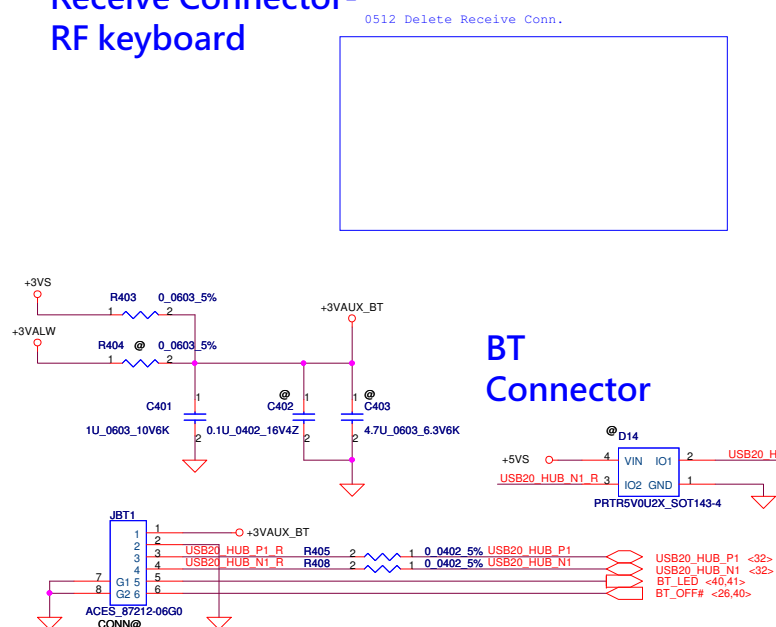
Mini Card Slot--WLAN



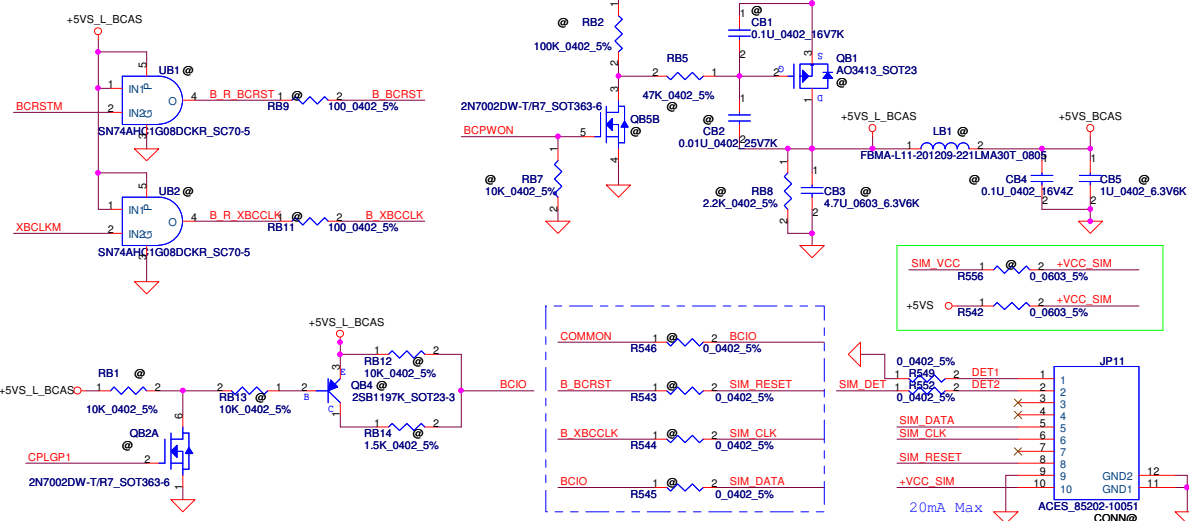
Mini Card Slot 1---TV tuner Currecnt: 3.3 : 1000mA, 1.5: 500mA



Receive Connector-
RF keyboard



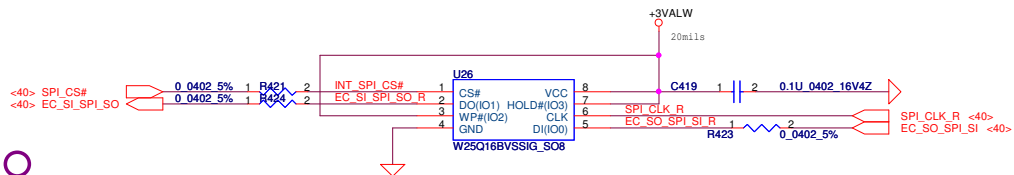
B-CAS Circuit



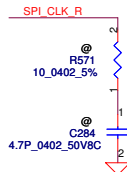
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SPI Flash (16Mb*1)

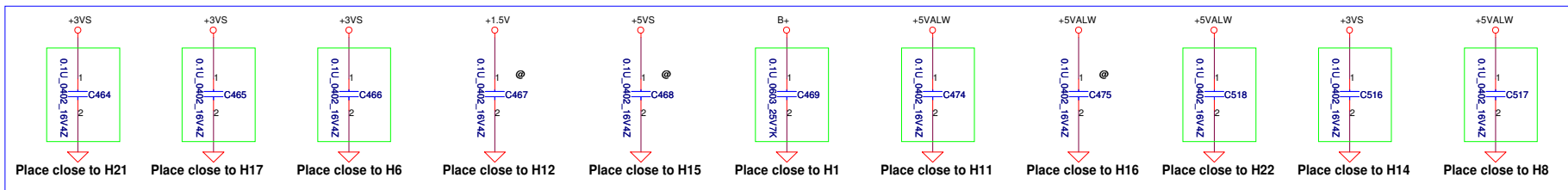
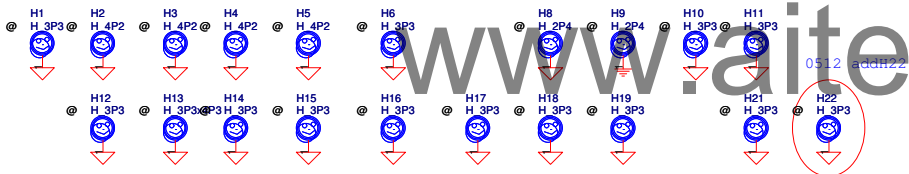
Change U26 P/N from SA000041N00 to SA00002T000 0518
0707 Change U26 P/N from SA00002T000 to SA00003F000
Change U26 symbol



Place closely pin 6



Screw Hole



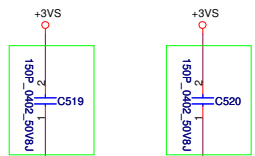
0709 Change C464/C465/C466 from @ to mount

Reserve for ESD request 0503

Change C469 from 16V to 25V

0709 Change C474/C516/C517 from @ to mount

0709 Add C518 for ESD request

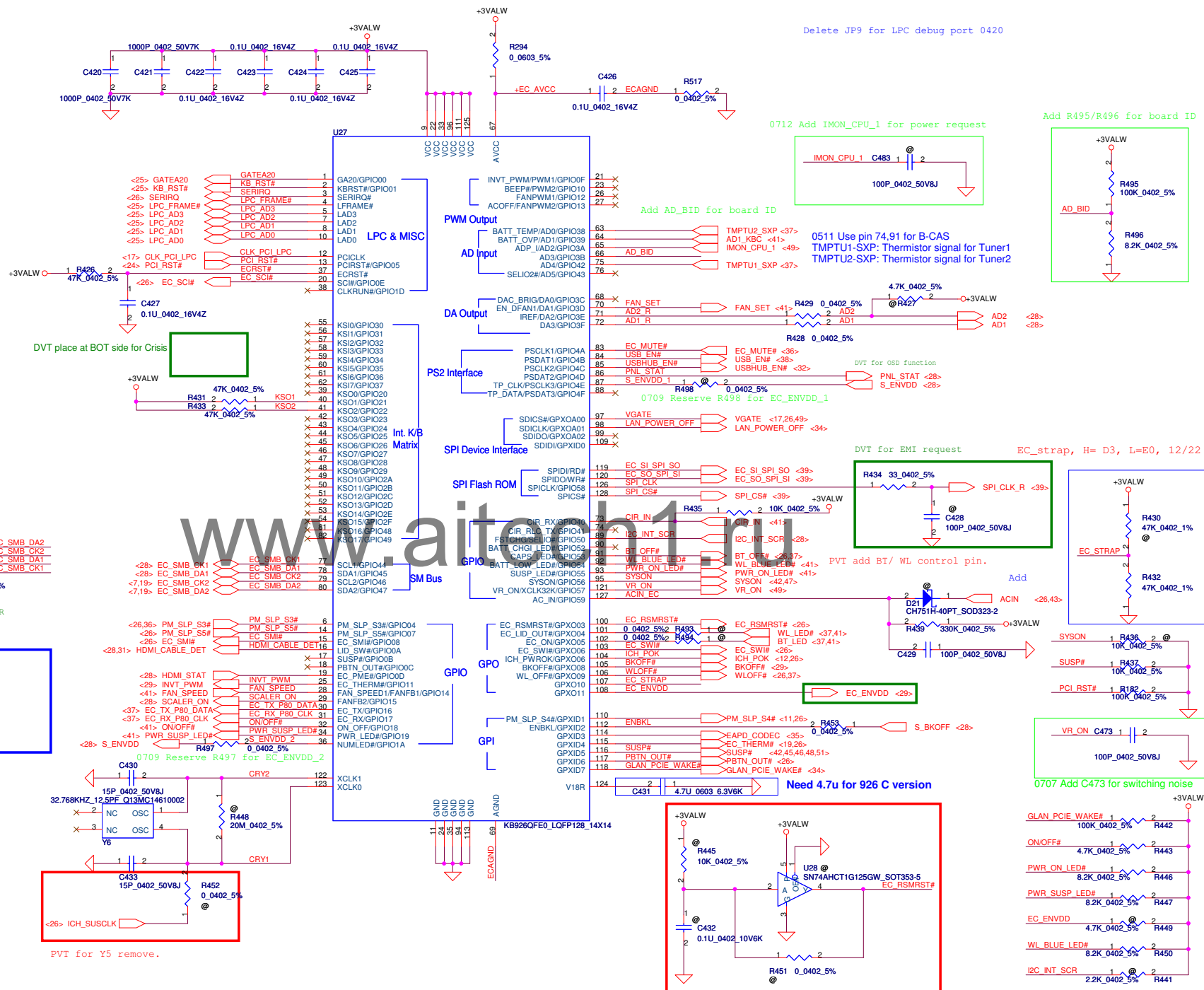


Place close to H21

Place close to H17

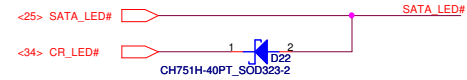
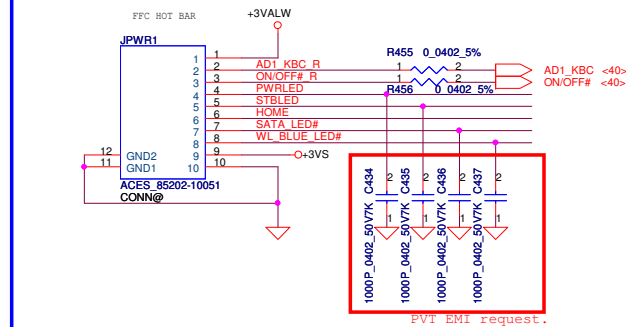
0709 Add C519/C520 fro ESD request

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				Size	Document Number
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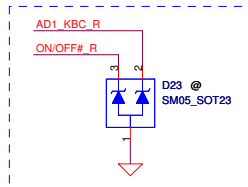


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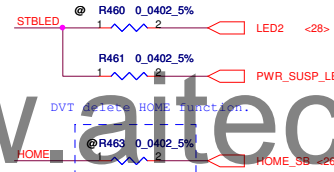
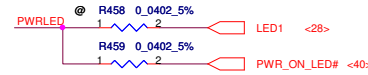
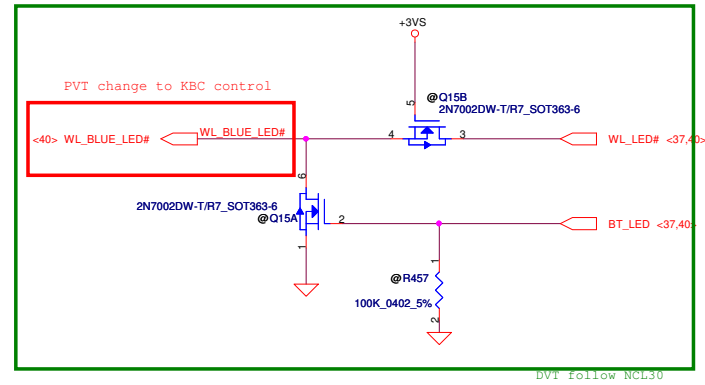
Power switch board



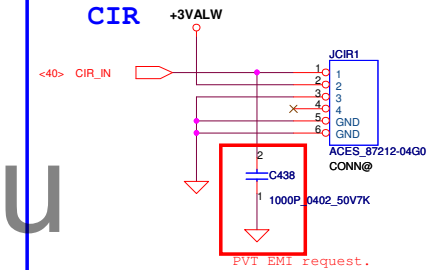
For ESD request, close to JPWR1



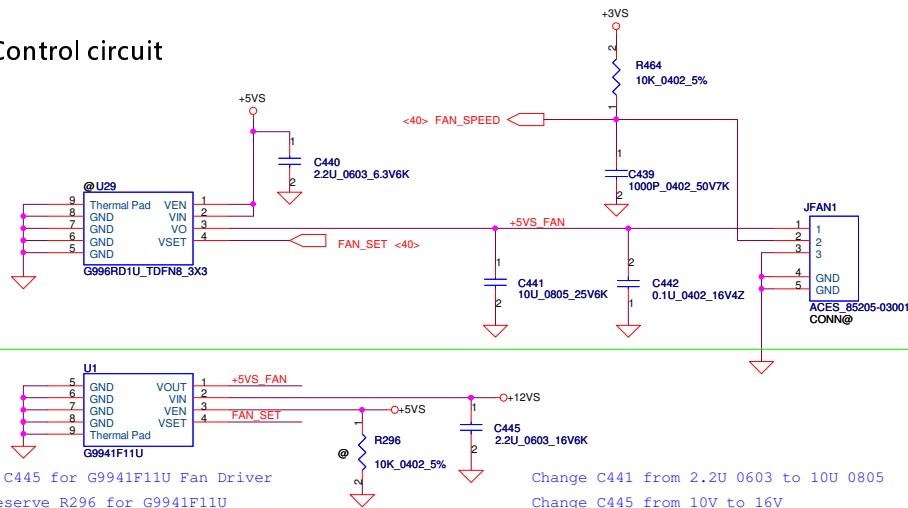
WLAN and BT LED inform pin to KBC



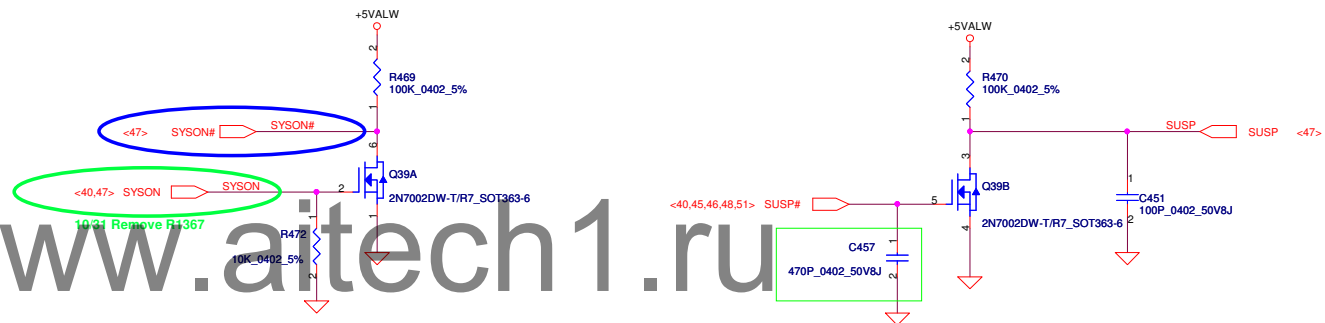
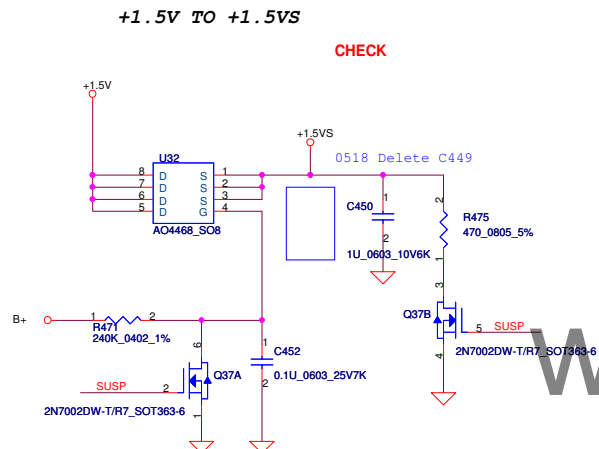
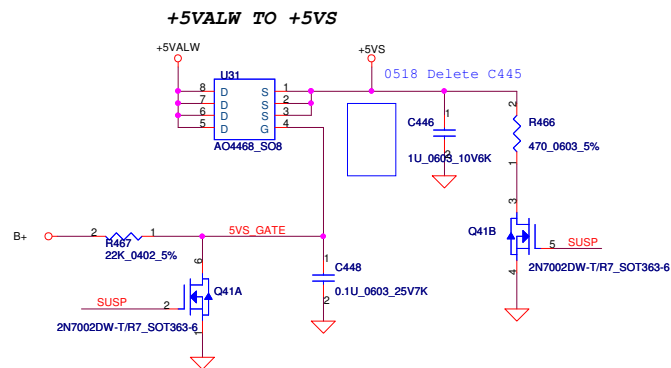
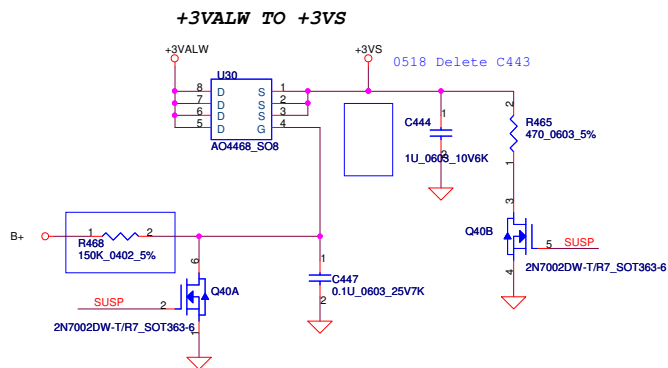
CIR



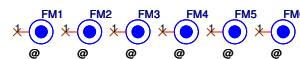
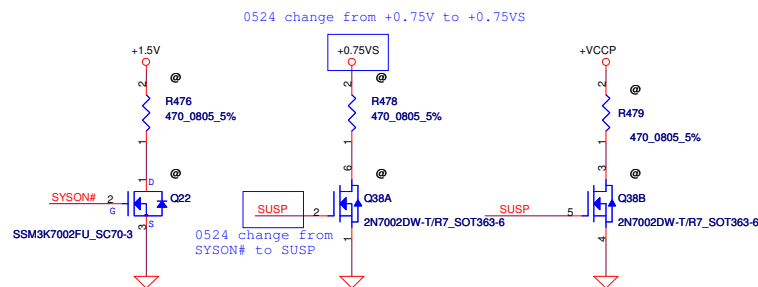
Fan Control circuit



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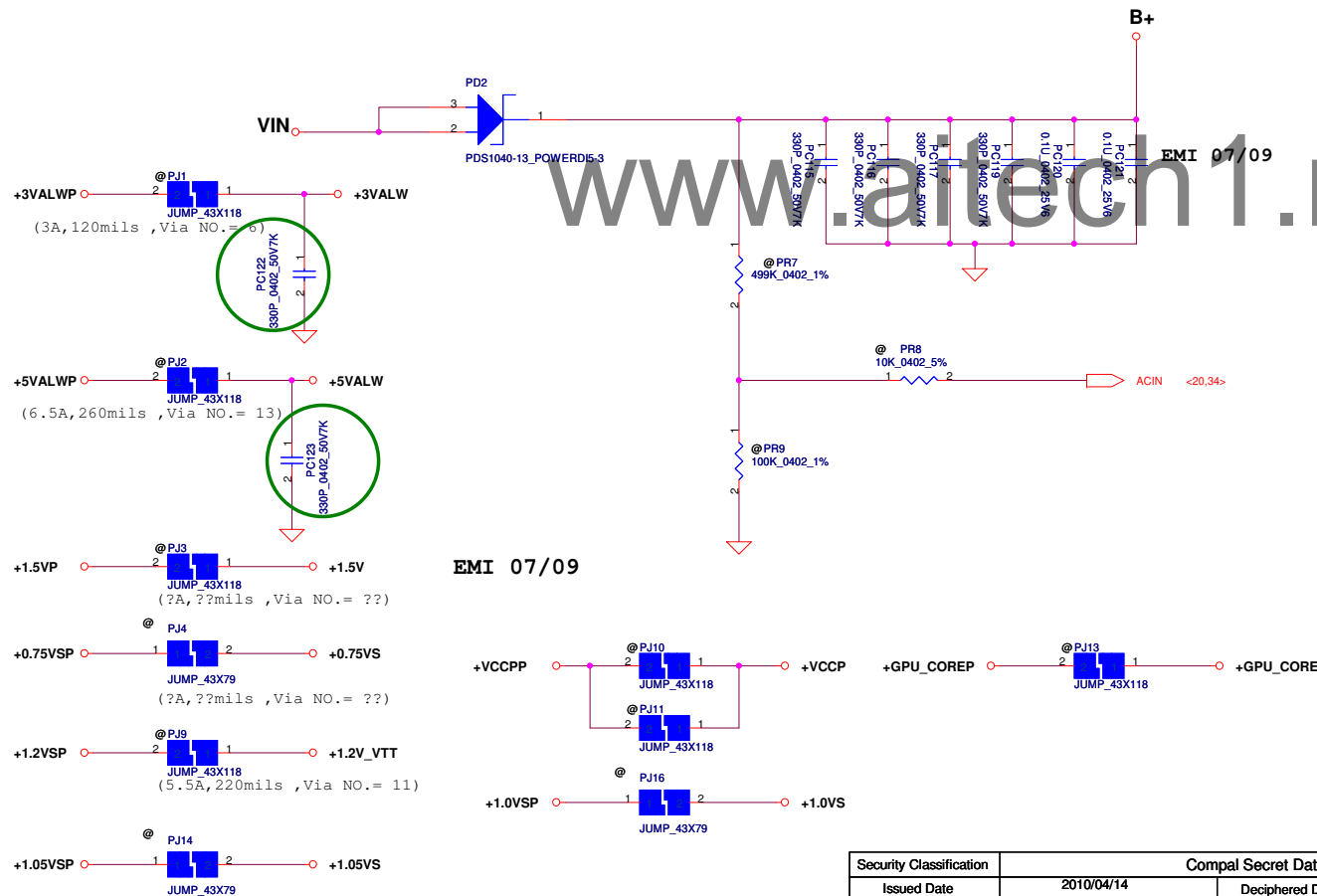
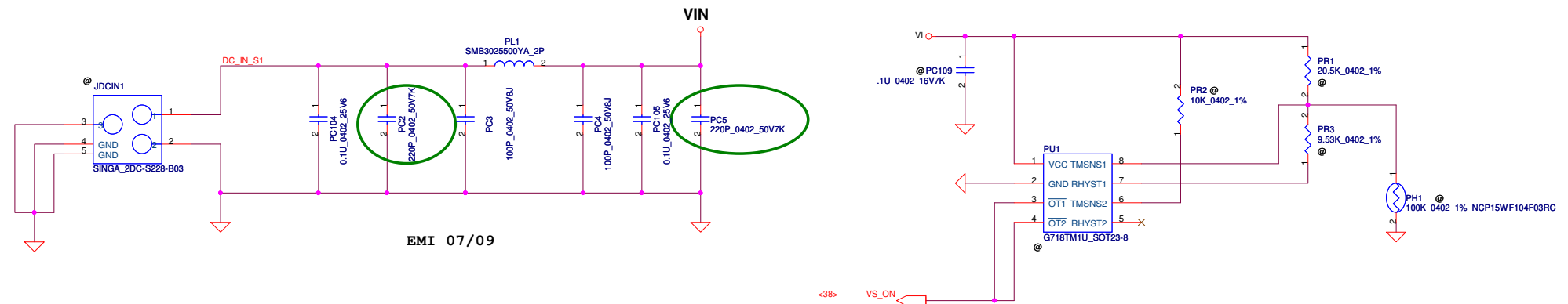
Discharge circuit



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PH1 under CPU botten side :

CPU thermal protection at 92 degree C
Recovery at 57 degree C

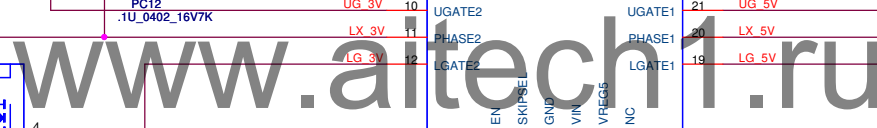


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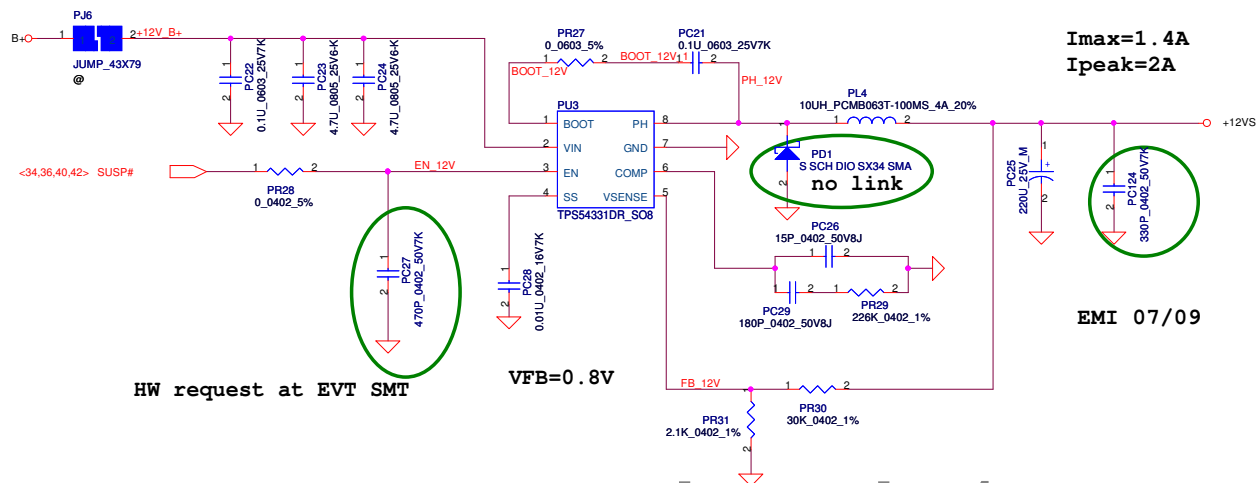
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$I_{max}=3.87A$
 $I_{peak}=5.53A$
 $I_{ocp}>=1.2 \cdot I_{peak}=6.64A$
 $I_{ocp}=10A$

```
Rds (ON) :Max=16.5m-ohm
           Min=13.5m-ohm
           Imax=6.4A
           Ipeak=9.15A
           Iocp>=1.2*Ipeak=11.16A
           Iocp=12A
fsw=300kHz
OCP=200k/16.5m=12
```

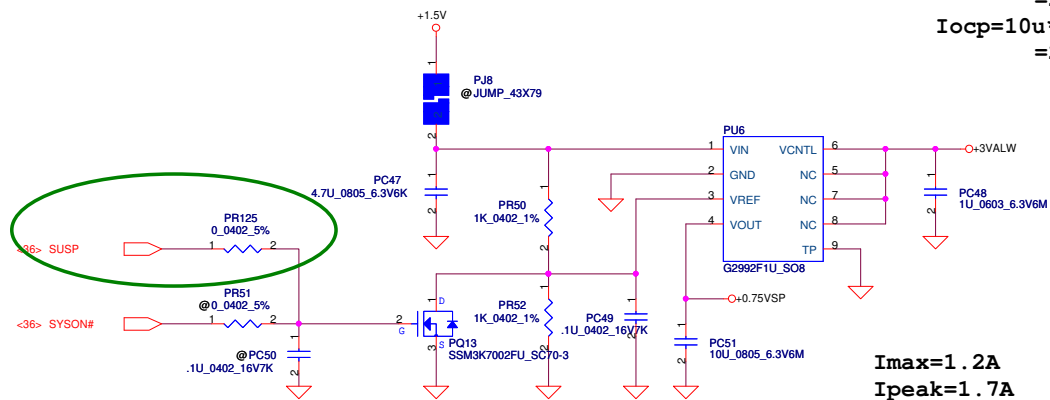
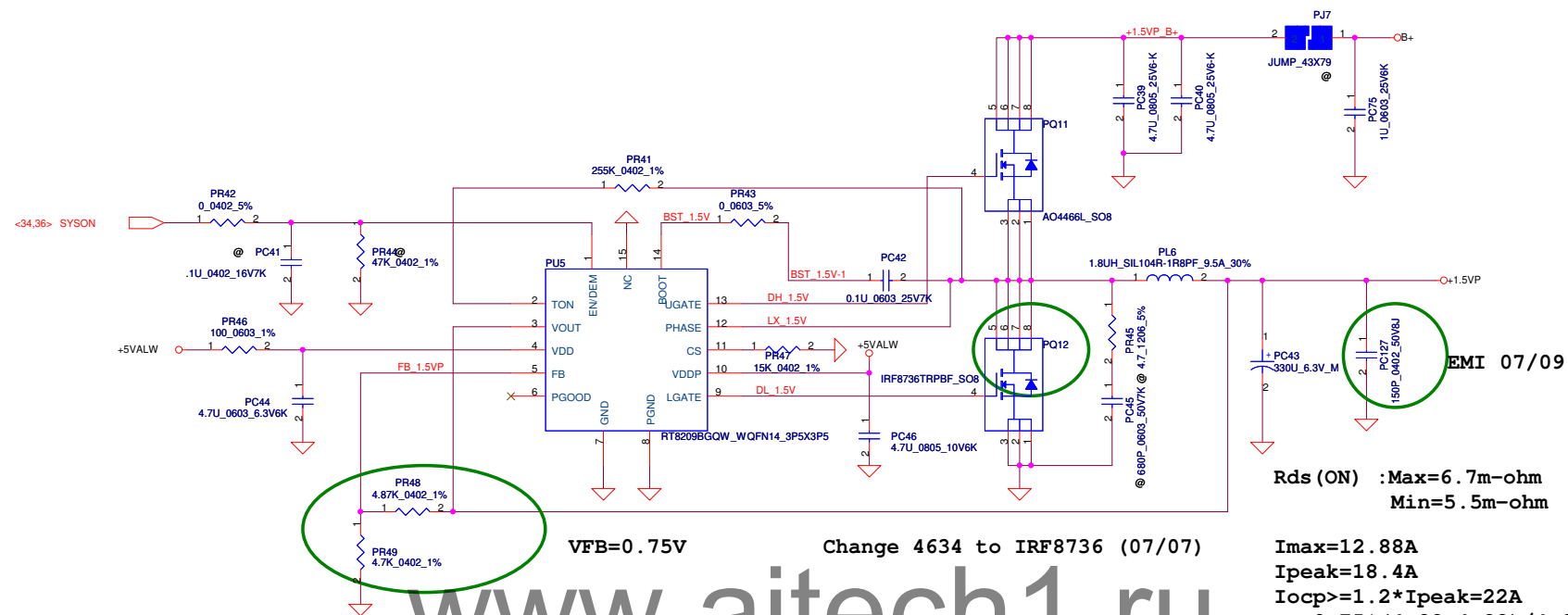


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Confirm with Joe
add pull down 10k
06/29

choke DCR:1.33m-ohm
Iocp=3*96u*Rsense/DCR
=>Iocp=0.217*Rsense
Iocp=0.217*412-ohm=89.4A

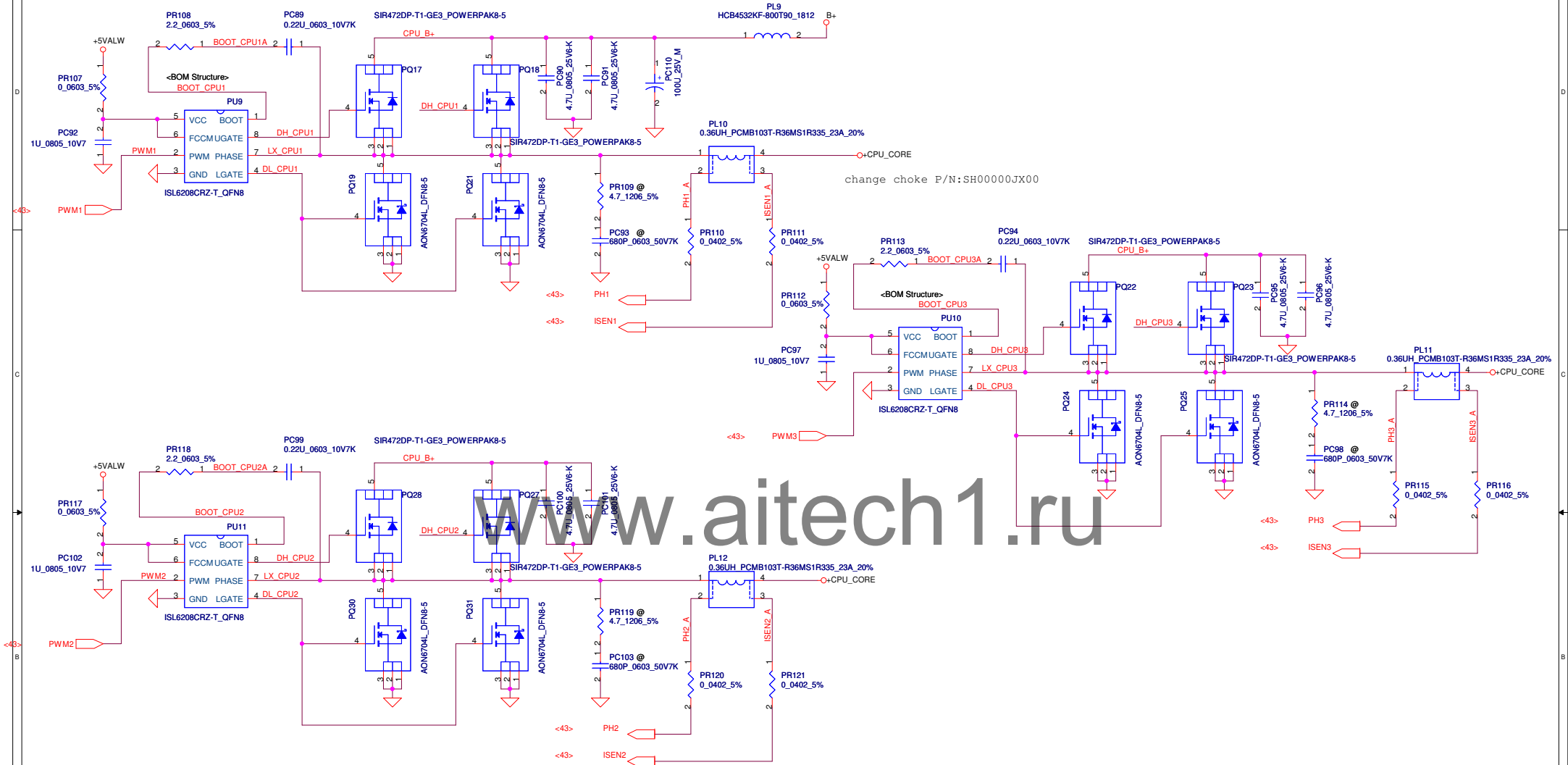
Base on test at
intersil
change 22k to
23.7k (06/29)

need mount
if this pin
floating, it
will impact
the OCP
setting

Load Line=1.7m-ohm
Need change to 1.82k-ohm for 1.7m-ohm test result
base on test at intersil, change 1.82k to 1.27k (06/29)
Change PC88 from 22p to 33p (06/29)

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change input cap P/N:SF000001280



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Item	Fixed Issue	Reason for change	PG#	Modify List	Remark	Date	Phase
1		Add X76 for APW7138 and ISL6268		Change PU7 to PU500 Change PC64 to PC900	X7619688L03 for APW7138	2010/04/29	EVT
2		Add +GPU_CORE, 1.8VS and 1.0VS power rail for DIS		Add RT8209B for +GPU_CORE Add SY8033 for 1.8VS Add APL5930 for 1.0VS		2010/05/03	EVT
3		Shortage problem		Change PQ12 from AO4456[SB000009F80] to SI4634[SB00000DA00] Change PQ9, PQ11, PQ29 from AO4466[SB00000CG00] to AO4466L[SB00000CG80]		2010/05/14	EVT
4		Shortage problem		Change PQ14 from SI7686[SB000008L80] to SIR472[SB00000K300]		2010/05/14	EVT
5		Shortage problem		Change PQ17, PQ18, PQ22, PQ23, PQ27, PQ28 from SI7686[SB000008L80] to SIR472[SB00000K300]		2010/05/14	EVT
6		cost down		Reserve PC27, PC23, PC202, PC41, PC50, PC106		2010/05/19	EVT
7		sequence risk		Change the ISL6334A and ISL6208 VCC from +5VS to +5VALW		2010/05/19	EVT
5		CPU PSI#		Add PR89 (10k-ohm) Delete PR88 (0 ohm)		2010/05/20	EVT
6		HW sequence Change 0.75V to 0.75VS		Add PR125 (0-ohm) Delete PR51 (0 ohm)		2010/05/24	EVT
7		Output voltage modify(up 1.5~2%)		Change PR40 from 4.99k to 6.04k Change PR39 from 3.01k to 3.83k Change PR49 from 4.99k to 4.7k Change PR48 from 4.99k to 4.87k Change PR151 from 20k to 20.5k Change PR134 from 2.49k to 2.61k Change PR62 from 4.22k to 4.32k Change PR255 from 1.58k to 1.69k		2010/05/31	EVT
7		Modify HW power sequency		Change PR33 from 0 to 300k Change PR130 from 0 to 200k Change PR139 from 0 to 47k Change PR152 from 0 to 249k Add PC33, PC106, PC158, PC166 0.1uF			

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